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Data Retention Characteristics of MONOS Devices with High-*k* Dielectrics and High-work Function Metal-gates for Multi-gigabit Flash Memory

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1. Introduction

Silicon/metal-oxide-nitride-oxide-silicon (SONOS/MONOS) devices receive increasing interest recently due to their simpler process, smaller cell size, and better endurance over the floating-gate devices [1]. However, charge retention and erase speed remain as the major challenges for SONOS devices to replace floating-gate devices [1,2]. Recently, it is reported improved erase performance and endurance characteristics can be achieved by replacing SiO_2 and poly-Si as high-k dielectric, Al_2O_3 and high-work function metal, TaN for blocking oxide and gate material, respectively [3]. However, data retention characteristics still need to be improved since memory window is very small after long time retention. In this work, we present an optimized cell structure for both improved data retention and erase speed in SONOS-type flash EEPROM.

2. Experimental

The fabricated TANOS cells consist of TaN/Al_2O_3/Si_3N_4/ tunnel oxide/*p*-Si (TANOS). Table I shows the process flow of the TANOS devices. Al_2O_3 was deposited by atomic layer deposition using Trimethylaluminum ($Al(CH_3)_3$) and O_3, followed by post-deposition anneal at 950°C. TaN film was deposited by MOCVD at 500°C with the thickness of 160 Å and n+ poly-Si was deposited on top of the TaN layer. Figure 1 shows the cross-sectional TEM image of the fabricated TANOS cell.

Table I Key process flow of TANOS devices

-V_{th} adjustment implant and gate oxide formation (40 Å)
-Silicon nitride deposition by LPCVD (65 Å)
-Al_2O_3 deposition (100, 150, 200 Å) by ALD
-TaN deposition by MOCVD
-N+ Poly-silicon deposition
-Gate definition (lithography and etching)
-N+ S/D implant

3. Results and Discussion

Figures 2 and 3 show program and erase characteristics of fabricated TANOS devices for various blocking oxide thickness. The same electric field of 14 MV/cm (-14 MV/cm for erase) was applied to the devices. The program and erase speeds become faster as the blocking oxide thickness increases. When blocking oxide thickness increases, lower leakage current and higher breakdown field can be obtained even at the same electric field due to reduced electron back tunneling from the gate.

For multi-gigabit flash memory it is critical to obtain wide operating voltage windows to separate program and erase states. Figures 4 and 5 show the operating voltage windows for both program and erase states. With 200 μs programming and 2 ms erasing as blocking oxide thickness increases the amount of flatband voltage (V_{FB}) shift is higher and operating voltage windows are larger due to higher dielectric breakdown voltage and lower leakage current.

The charge retention characteristics of TANOS devices (O/N/A=40/65/100 Å) are investigated in a temperature range from 200°C to 275°C. The time to failure (t_F) at different temperatures is expressed as

$$t_F = const./R = const.\times\exp(E_a/kT)$$

or $\ln t_F = const. + E_a/kT$.

(E_a is the activation energy (in eV) of the process, k is the Boltzmann constant, and T is the temperature in Kevin.) Figure 6 shows the plot of the ln t_F vs. $10^3/T$. The lifetime activation energy of 1.17 eV was obtained. A prediction of the retention performance derived from the activation energy is shown in Fig. 7. At this rate, it takes longer than 40 years at 85°C to achieve a 0.5 V loss from the initial programmed state.

Data retention characteristics of TANOS devices with different blocking oxide thickness are shown in Fig. 8. Bake retention test was performed at 250°C for 2 hours. As blocking oxide thickness increases, the charge loss is reduced. There is only less than 0.2 V charge loss for a device with 200 Å-thick-blocking oxide. This fact explains that trapped electrons can be lost through blocking oxide as well as tunnel oxide. From the results, it is confirmed that the thicker blocking oxide gives us better endurance and data retention properties.

4. Conclusions

The effects of blocking oxide thickness on the program/erase speed and data retention characteristics in TANOS devices were demonstrated. By employing high-*k* dielectrics and high-work function metal gates, a large memory window of over 6 V and less than 0.2 V charge loss at high-temperature bake test have been obtained. Therefore, the fabricated TANOS devices show one of the most promising candidates for future flash EEPROM.

References

[1] M. H. White, D. A. Adams, and J. Bu, *IEEE Circuits and Devices* **16** (2000) 22.
[2] S.-I. Minami and Y. Kamigaki, *IEEE Trans. Electron Dev.* **40** (1993) 2011.
[3] C. H. Lee et al., *IEEE Electron Devices Meeting* (2003) 613.

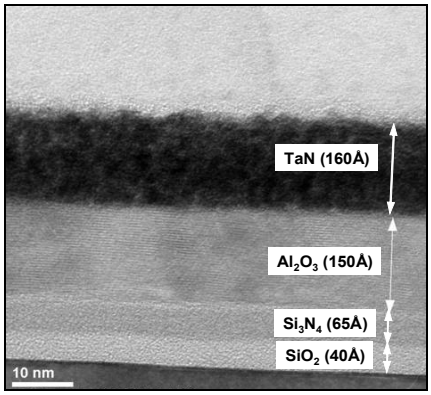

Fig. 1. Cross-sectional TEM result of fabricated TANOS device.

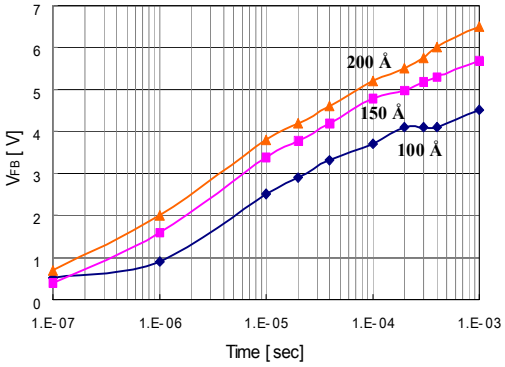

Fig. 2. Program characteristics for different blocking oxide thickness with the same program electric field of 14 MV/cm.

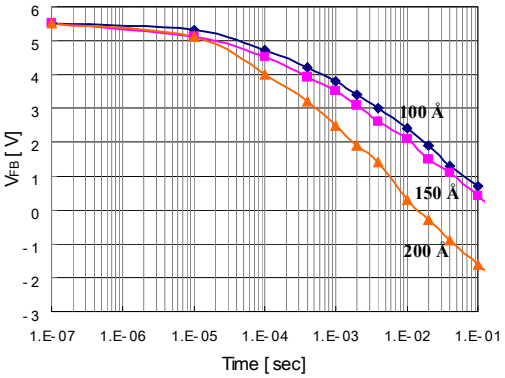

Fig. 3. Erase characteristics for different blocking oxide thickness with the same erase electric field of -14 MV/cm.

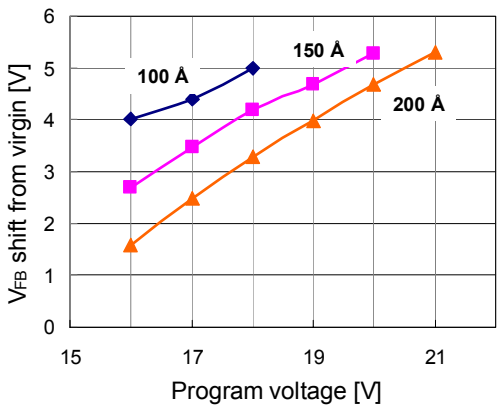

Fig. 4. Operating program window with different blocking oxide thickness according to applied bias after 200 μs program time.

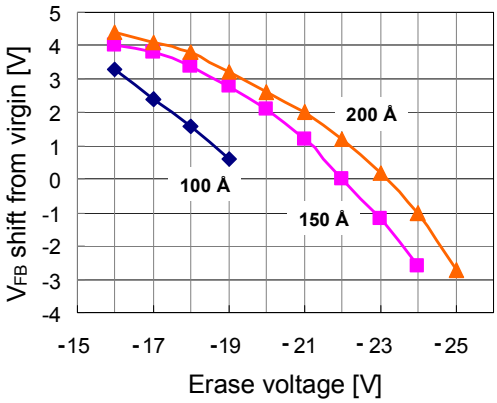

Fig. 5. Operating erase window of the TANOS devices after 2 ms erase time.

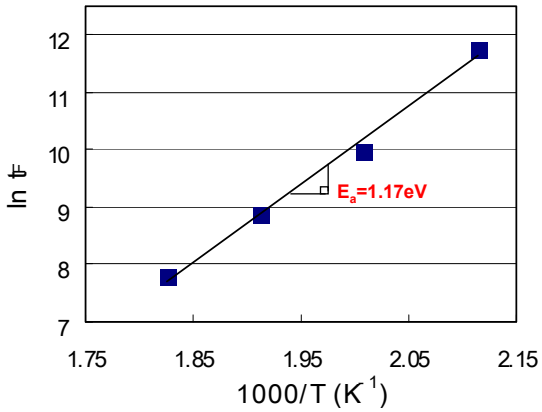

Fig. 6. Lifetime activation energy calculation.

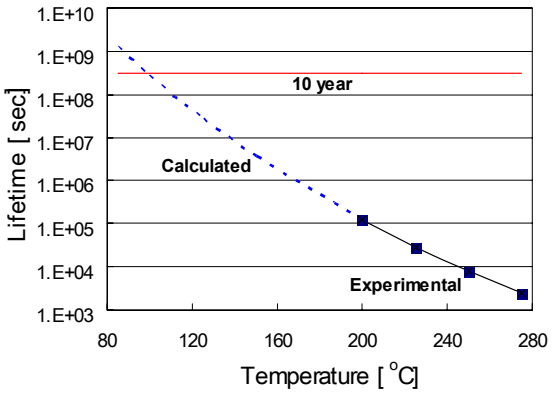

Fig. 7. Prediction of lifetime in terms of bake retention.

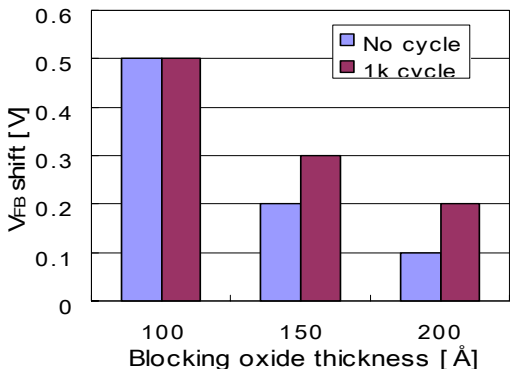

Fig. 8. Comparison of the data retention characteristics with and without cycling stress for various blocking oxide thickness.