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H-3-2

Highly Reliable and Manufacturable Low-Temperature Plasma Assisted Oxidation for High Density SRAM with Double Stacked Cell Structure

C.-S. Kim, Y. J. Noh, J. H. Kim, B. Y. Koo, J. H. Heo, D.-C. Kim, Y. G. Shin, U-In Chung, and J. T. Moon
Memory Division, Samsung Electronics Co., Ltd. San#24, Nongseo-Ri, Giheung-Eup, Yongin-City, Gyeonggi-Do, Korea
Tel: +82-31-209-1365, FAX: +82-31-209-6299, E-mail: chulsung.kim@samsung.com

1. Introduction

The S^3 SRAM cell with stacked cell transistors (Stacked Single-crystal Thin Film Transistor, SSTFT) was developed to integrate the highest density of SRAM [1-3]. The S^3 SRAM suffered from severe degradation of short channel effect (SCE) due to much thermal budget to fabricate the pass nMOSFET (PSTR) and the load pMOSFET (LDTR), which should be formed on the ILD layers to reduce the cell areas. In this study, low-temperature plasma oxidation process to fabricate the gate dielectric and gate poly-silicon re-oxidation, which requires the highest thermal process, of stacked LDTR and PSTR on the ILD layers is applied to improve the SCE of planar pull-down transistors (PDTR) and core peripheral logic circuits in double stacked device. Improved SCE in addition to excellent reliability such as Q_{BD}, TDDB and NBTI compared to thermal oxide will be discussed.

2. Experimental

Key processes for the fabrication of 80nm S^3 SRAM with double stacked cell structure are summarized in Fig. 1. The PDTR and core peripheral circuits are made on bulk Si substrate because these transistors need the best performance among three transistors for SRAM cell as shown in Fig. 2. The PSTR is stacked over LDTR which already stacked on the PDTR. To fabricate this stacked SRAM cell, triple times of gate dielectric formation and gate poly-silicon re-oxidation are needed. The repeated oxidation process can deteriorate the SCE characteristics of the PDTR and core peripheral transistors on bulk silicon. So, the low-temperature plasma oxidation was designed to grow plasma oxide followed by plasma nitridation (PN) processes using microwave-excited plasma system at 400℃ to improve SCE characteristics. Thermally grown silicon oxide film was formed by wet oxidation at 950℃ followed by plasma nitridation with RF power source and post nitridation anneal (PNA) as a reference sample.

3. Results and discussion

A. Transistor Characteristics with plasma oxide

The device has three times of oxidation for gate oxide and gate poly-silicon re-oxidation to produce triple layers for cell structure. Fig. 3 shows the roll-off behavior of peripheral transistors having four steps of the thermal annealing, 2^{nd} gate oxidation, 2^{nd} gate poly-silicon re-oxidation, 3^{rd} gate oxidation and 3^{rd} gate poly-silicon re-oxidation. Plasma oxidation process shows the well-behaved V_{th} roll-off characteristics compared to thermal oxide, which is due to its low temperature process. Fig. 4 shows V_{th} variation of core peripheral n,pMOSFETs between thermal oxide with high temperature process and plasma oxide with low temperature process. V_{th} of nMOSFETs with plasma oxide is higher than that of thermal oxide. On the other hand, pMOSFET's V_{th} is also lower than that of thermal oxide. It is also found that these differences in V_{th}'s for n,pMOSFETs is attributed to oxidation process between thermal oxide and plasma oxide as shown in Fig. 5. Fig. 6 shows C-V plots for the two gate dielectrics, which show low V_{th} for thermal oxide in nMOSFET. The differences in V_{th} can be explained by flat band voltage shift as well as different doping profile coming from different thermal budget. The less flat band voltage shift of plasma oxide is due to thin transition layer, which has many defect sites such as dangling bonds, strained bonds, interface traps and fixed charges. The drain current of n,pMOSFETs with plasma oxide is similar to that of thermal oxide irrespective of plasma nitridation as shown in Fig. 7. Fig. 8 shows transistor characteristics of PSTR in stacked SRAM cell. As it can be seen, the swing characteristics of PSTR with plasma oxide for gate dielectric and gate poly-silicon re-oxidation is comparable to the planar bulk transistor in spite of low-temperature plasma oxidation. Field effect mobility for different gate dielectrics is compared in Fig. 9, where plasma oxide has a little reduced mobility compared to thermal oxide. The reduced mobility is assured to be due to channel-ion implanted damages, which have not been cured by low thermal treatment.

B. Characteristics of low temperature plasma oxide

Fig. 10 shows J_G-V_G curves for thermal oxide and plasma oxide for stacked SRAM. The plasma oxide shows lower leakage current than thermal oxide regardless of post thermal treatment for stacked SRAM Cell. The charge-to-breakdown (Q_{BD}) characteristics for the plasma oxide is superior to that for thermal oxide, and plasma oxide with plasma nitridation is equivalent to that of thermal oxide with plasma nitridation in spite of skipping PNA for plasma oxide (Fig. 11). The plasma oxide has the better time dependent dielectric breakdown (TDDB) irrespective of post thermal budget for stack process as shown in Fig. 12. Fig. 13 shows the negative bias temperature instability (NBTI) characteristics of pMOSFET for oxide with plasma nitridation, which also presents the longer NBTI characteristic for plasma oxide. It is assured that the superior effects of plasma oxide are due to thin transition layer of plasma oxide which degrades the electrical property [4]. Fig. 14 shows O/Si ratio in silicon dioxide grown by plasma thermal oxidation, which is measured by X-ray photoelectron spectroscopy (XPS). The O/Si ratio in plasma oxide is more stoichiometric than that in thermal oxide. These results imply that plasma oxidation is highly reliable and manufacturable oxidation process despite of low-temperature oxidation process. In terms of reliability and low thermal budget, the plasma oxidation is expected to be very promising process for the formation of an ultra-thin gate dielectric for stacked cell structure.

4. Conclusion

Ultimately ultra-low thermal budget solution with plasma oxide process for gate dielectric and gate poly-silicon re-oxidation is successfully developed for stacked cell structure of SRAM for the first time. The SCE of core and peripheral logic circuits of SRAM is effectively improved by employing plasma oxide. In addition, the dielectric properties related with reliability such Q_{BD}, TDDB and NBTI were improved by plasma oxidation. The plasma oxidation technology is a promising candidate as a gate dielectric formation and gate poly-silicon re-oxidation technology for sub-80 nm stacked structure devices.

References

[1] Soon-Moon Jung et al., VLSI Symp. Tech. Dig., p. 228, 2004
[2] W.S. Cho et al., Extended Abstracts SSDM, pp. 190-191, 2004
[3] Soon-Moon Jung et al., IEDM Tech. Dig., p. 265, 2004.
[4] S. Hyun et al., Appl. Phys. Lett. 85(6), p. 988, 2004.

- **PDTR & CORE PERIPHERAL**
- STI, well & Vth adjust implantation
- *1st gate oxidation(35Å) & plasma nitridation*
- 1st gate poly-silicon
- *1st gate poly-silicon re-oxidation*
- LDD I/I & spacer, n+, p+ source/drain
- 1st ILD1 & ILD1 CMP
- **LDTR**
- single crystal channel Si for LDTR
- *2nd gate oxidation(35Å)* & gate poly-silicon
- *2nd gate poly-silicon re-oxidation(27Å)*
- LDD, spacer, P+ S/D and RTA and CNT
- **PSTR**
- single crystal channel Si for PSTR
- *3rd gate oxidation (35Å)* & gate poly-silicon
- *3rd gate poly-silicon re-oxidation (27Å)*
- LDD, Spacer, N+ S/D, RTA and CNT

Fig. 1: Key processes for S^3 SRAM.

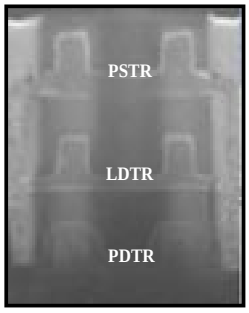

Fig. 2: Cross sectional SEM image of the double stacked S^3 cell.

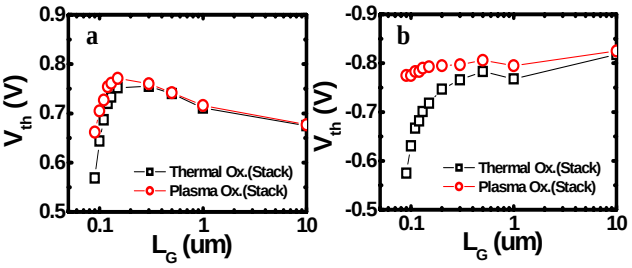

Fig. 3. SCE characteristics for the different thermal process of gate dielectric and gate poly-silicon re-oxidation of double stacked SRAM cell: a) nMOSFETs, b) pMOSFETs.

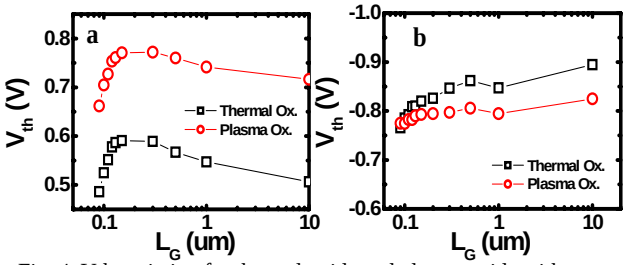

Fig. 4. Vth variation for thermal oxide and plasma oxide with each plasma nitridation under the same post- thermal treatment: a) nMOSFETs, b) pMOSFETs.

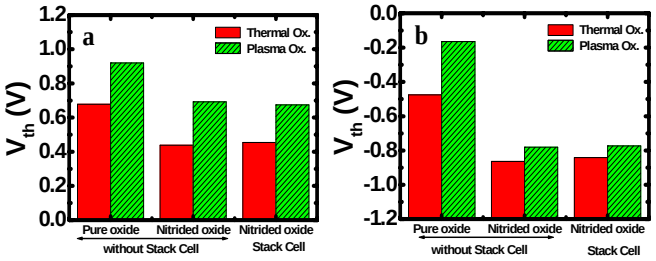

Fig. 5. Vth variance for pure oxide and nitrided oxide without stacked SRAM cell and for nitrided oxide with stacked SRAM cell: a) nMOSFE, b) pMOSFET.

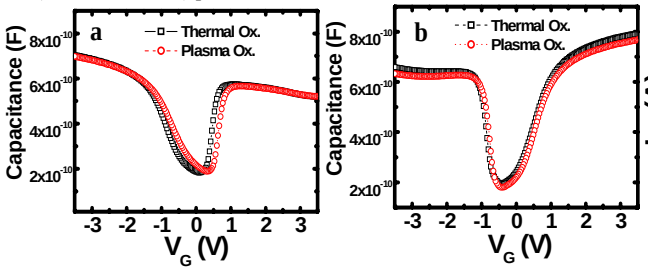

Fig. 6. C-V plots of plasma oxide and thermal oxide with plasma nitridation: a) nMOSFETs, b) pMOSFETs

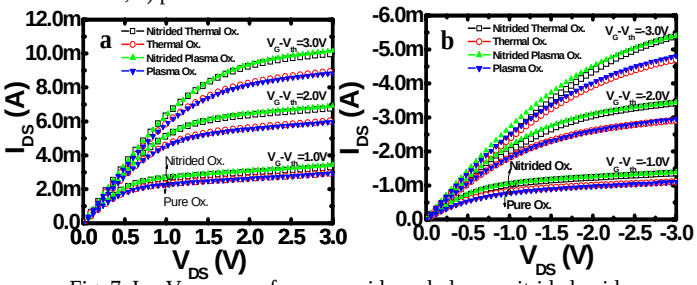

Fig. 7. I_{DS}-V_{DS} curves for pure oxide and plasma nitrided oxide (W/L =10./0.10 (um/um)): a) nMOSFET, b) pMOSFET

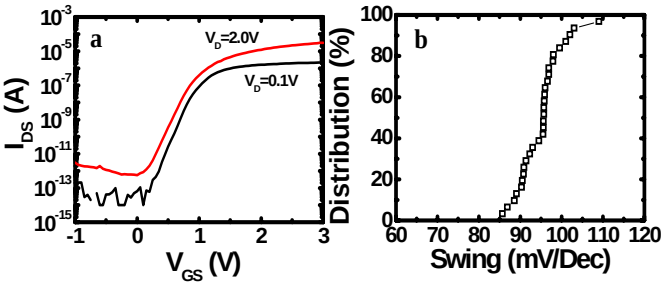

Fig. 8. PSTR characteristics of stacked SRAM Cell: a) I_{DS}-V_{GS} curve, b) Swing distribution.

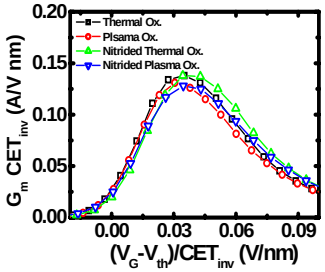

Fig. 9. Mobility of thermal oxide and plasma oxide both pure oxide and plasma nitrided oxide

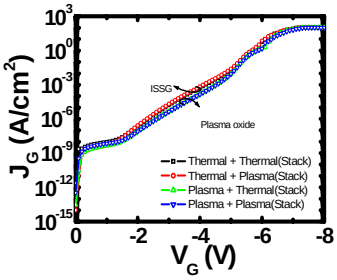

Fig. 10. J_G-V_G curves for thermal oxide and plasma oxide for stacked SRAM cell process.

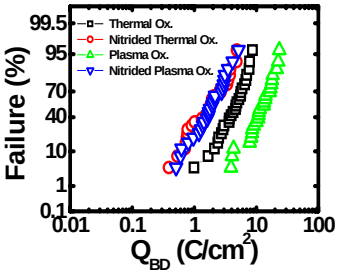

Fig. 11. Charge-to-breakdown (Q_{BD}) characteristics for thermal oxide and plasma oxide

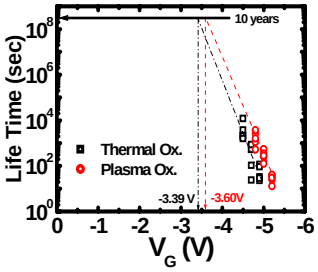

Fig. 12. TDDB life time of two gate dielectrics with different thermal budget.

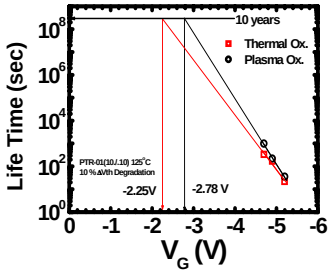

Fig. 13. NBTI life time of pMOSFETs for thermal oxide and plasma oxide

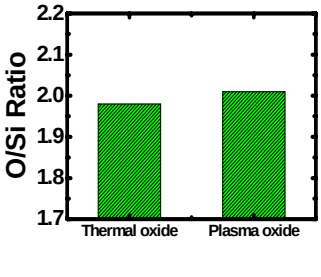

Fig. 14. O/Si ratio in thermal oxide and plasma oxide