Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.446-447

H-4-2

Impact of Vth interference suppression using a novel Poly Si shield on FLASH memories.

T. Fukumura, S. Shimizu, Y. Ikeda, M. Shimizu, M. Fujinaga, K. Ishikawa
F. Ohta, A. Fukasawa, T. Yoshitake, K. Hirao, O. Tsuchiya and Y. Ohji
Renesas Technology Corp., 4-1, Mizuhara, Itami-shi, Hyogo, 664-0005, Japan
Tel: +81-72-784-7356, Fax: +81-72-780-2693, E-mail: fukumura.tatsuya@renesas.com

1. Introduction

The flash memory for mass storage applications such as digital camera and MP3 player has been intensively developed, because there is a great demand for low-cost and high-density memories in recent years. As scaling of the memory cell size is decreasing, the parasitic capacitance between the memory cell and adjacent memory cells is increasing. As a result, Vth of the memory cells are affected by the change of Vth of adjacent memory cells when they are programmed or erased. The influence of adjacent memory cells is called “Vth interference”. To suppress this Vth interference is more important for multi-level cell (MLC) than single-level cell (SLC), because Vth distribution of MLC is required more limited than that of SLC.

In this paper, we demonstrate that the narrow Vth distribution can be realized to suppress Vth interference using a novel poly Si shield (PS).

2. Vth interference

Fig.1 shows the Vth distributions of AG-AND MLC. The width of each state must be kept narrow, because Vth distribution is divided into 4 states that need to have margins on both upper and lower sides for each state. Decrease of Vth interference is very important.

Vth interference is caused by parasitic capacitance coupling between adjacent memory cells. Fig.2(a) and (b) show the bird’s-view of proposed memory cell structure with PS and the conventional structure (without PS) of 90nm-node AG-AND type flash memory cells, respectively. Fig.3 shows the top down image of the AG-AND type flash memory cells.

3. Simulation Results

We estimate the effects of PS using 3-D Selete simulator [1]. Table 1 shows the influence of Vth interference from the each adjacent memory cell in the case of 90nm-node AG-AND. This table shows that Vth interference of the memory cells with common BL (2 and 8) are bigger than that of the memory cells with common WL (4 and 6), because there are only SiO2 between the memory cells with common BL, on the other hand, there are poly Si of Control Gate (CG) between the memory cells with common WL. Therefore, we investigate to decrease Vth interference by filling between WLs by poly Si.

Fig.4(a) and (b) show the dependence on the shape of PS, as a function of depth and width, respectively. Vth interference depends heavily on the depth than width of PS. These simulation results indicate that Vth interference decrease half making depth of PS 200nm from top of the Floating Gate (FG). As shown in Table1, Vth interference influenced by common BL memory cells decreases extremely, as we expected.

4. Experimental Results

Fabrication process applied to AG-AND type flash memory is indicated in table2. After the memory cells are formed [2], the gap between WLs is filled SiO_2 insulator and poly Si for PS. PS surrounding CG is removed in order to decrease the parasitic capacitance between WL and PS, finally. This fabrication process can be applied to AG-AND easily, because gates of peripheral transistors formed after memory cell formation. However, this process can be applied to NAND and NOR type flash memories in the same way.

Fig.5(a) and (b) show cross-sectional SEM images of the 90nm-node AG-AND applied PS. The depth from top of the FG is 250nm and the width is 20nm. Between PS and FG are insulated by about 25nm thickness SiO2.

Fig.6 shows the experimental results of Vth interference dependencies on the thickness of insulator between FG and PS. Vth interference is suppressed half, in case of 25nm insulator thickness. The suppression of Vth interference is saturated above the 50nm in thickness, since PS cannot be formed enough, because space between AGs is filled with insulator. These experimental results consist with simulation results.

Fig.7 shows that the dependence of Vth interference on the process rule. As memory cell size becomes smaller, the effect of PS becomes bigger. The Vth interference decreases extremely 1/3 in 65nm-node and more in 45nm-node with PS.

5. Conclusion

We demonstrate that Vth interference is suppressed half (0.2V to 0.1V) to apply PS to AG-AND type flash memory. The effects of decreasing Vth interference heavily depend on the depth of PS. This method is also effective for NAND and NOR flash memories.

6. References

[1] N. Kotani, in Proc. SISPAD 1998, pp.3-7, 1998.
[2] Y. Sasago et al., IEDM Dig, Tech. Papers, pp.823-826, 2003.

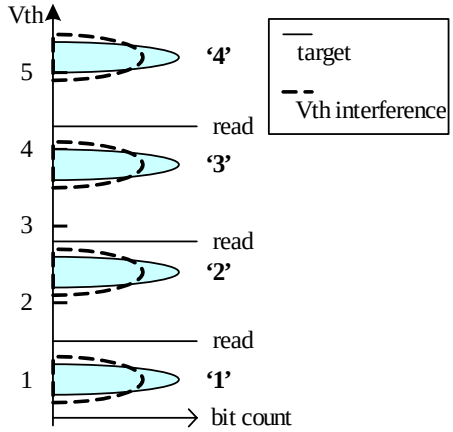


Fig.1. Vth distributions of AG-AND MLC

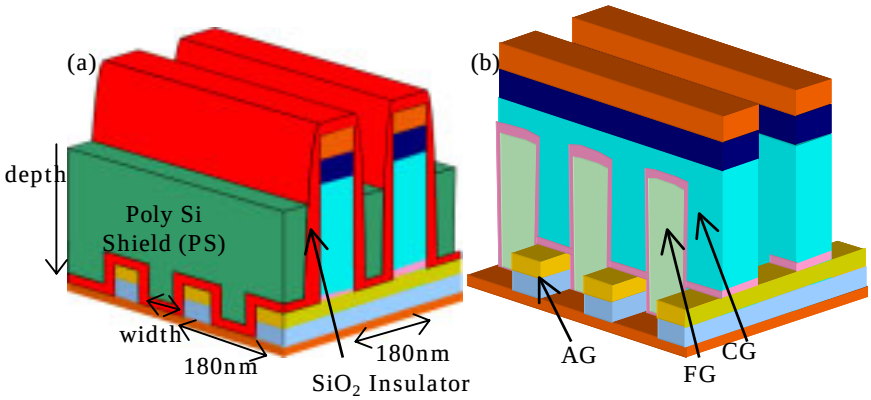


Fig.2. Bird's-eye views of 90nm-node AG-AND (a) with PS, (b) without PS (conventional)

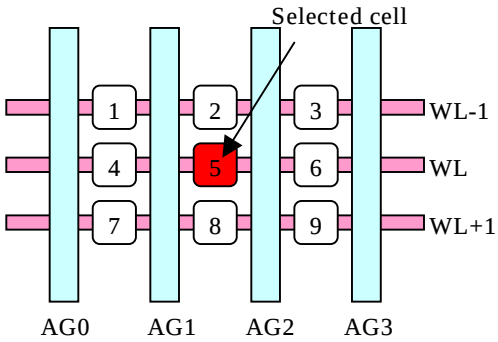


Fig.3. Top-down image, memory array of AG-AND flash memory.

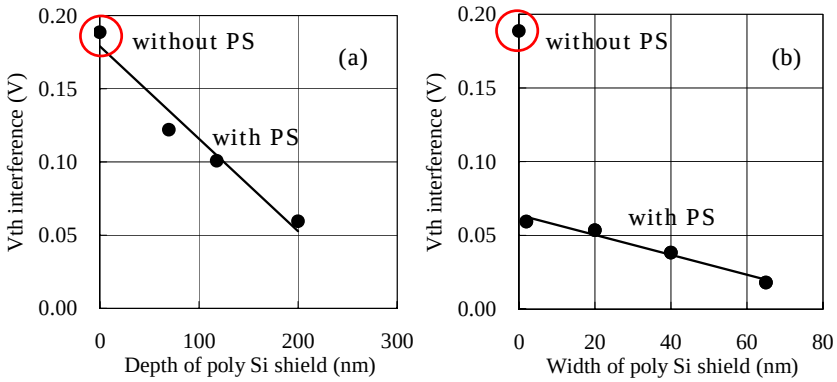
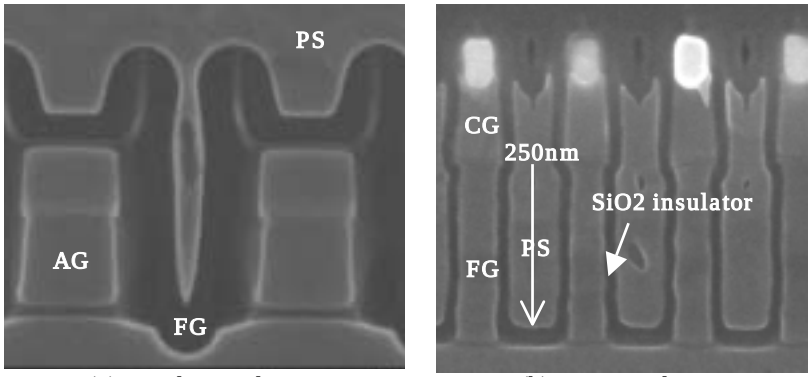


Fig.4. The simulated results of Vth interference dependencies on the shape of PS (a) as a function of depth, (b) as a function of width.

Table1. The influence of Vth interference from the adjacent cells in the case of 90nm-node AG-AND

	without PS (conventional)	with PS
cell 1 (diagonal)	3mV	1mV
cell 2 (common BL)	78mV	26mV
cell 3 (diagonal)	3mV	1mV
cell 4 (common WL)	10mV	5mV
cell 6 (common WL)	10mV	5mV
cell 7 (diagonal)	3mV	1mV
cell 8 (common BL)	78mV	26mV
cell 9 (diagonal)	3mV	1mV
Total	**190mV**	**64mV**



(a) Word-Line direction (b) Bit-Line direction

Fig.5. Cross sectional SEM of 90nm-node AG-AND with PS

Table 2. Fabrication process flow of AG-AND with PS

- STI formation
- Well implantation
- Assist Gate formation
- Floating Gate formation
- Control Gate formation
- ***Poly Si shield formation***
- Peripheral gate formation
- S/D implantation

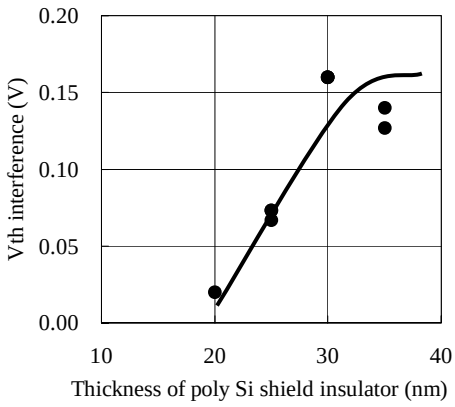


Fig.6. The experimental results of Vth interference as a function of insulator thickness.

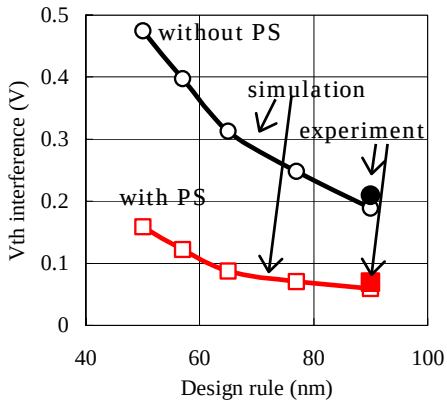


Fig.7. The dependence of Vth interference on design rule.