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Highly Reliable 256Mb NOR Flash MLC with Self-Aligned Process and Controlled Edge Profile

Wook Hyun Kwon , Jung In Han, Bomsoo Kim[1], Chang-Ki Baek[1], Sang-Pil Sim, Wook H. Lee, Jee Hoon Han, Cheol Jung, Heon Kyu Lee, Young Kwan Jang, Jeung Hwan Park, Dae Mann Kim[1], Chan-Kwang Park and Kinam Kim

Advanced Technology Development Team, Semiconductor R&D Center, Samsung Electronics Co., LTD.
San #24 Nongseo-Ri, Giheung-Eup Yongin-City, Gyeonggi-Do, Korea 449-711
[1] Korea Institute for Advanced Study, 207-43 Cheongryangri, Seoul, Korea
Tel) 82-31-209-8200 Fax) 82-31-209-3274, E-mail) wh.kwon@samsung.com

Abstract

We present a comparative investigation of two self-aligned processes, viz. Self-Aligned Poly (SAP) and Self-Aligned STI (SA-STI) for high-density flash memory cells. SAP is shown to lead to narrow erase Vth dispersion and better endurance reliability via the control of oxide edge profile. The erase Vth dispersion is systematically simulated vs. process variations, confirming the sensitive role of edge profile in affecting F-N tunneling current. We also present a successful operation of 256Mb NOR flash MLC, fabricated with a 90 nm technology by SAP process.

Introduction

To date, the cost per bit of flash memory has been reduced by two innovative approaches, viz. the design of Multi-Level Cell (MLC) and self-aligned process technology [1]. With the design of MLC the chip size can be reduced nearly by 40% without shrinking constraints of the process technology. The MLC operation, however, requires several process difficulties to be overcome for achieving small Vth dispersion and high reliability. Additionally, self-aligned processing is shown a key feature for shrinking the cell size. Recently, Self-Aligned Poly (SAP) and Self-Aligned STI (SA-STI) process schemes have been utilized for the scaling of flash cells [2]. In this paper, we show that the erase Vth dispersion, reliability and endurance characteristics are much improved by the control of the tunnel oxide profile at the STI edge. The reasons of these improvements via SAP are discussed, using TCAD simulation.

Process Architecture and Cell Structure

In Fig.1, the process flow diagram of SAP and SA-STI are shown. The SAP scheme [2] has key advantages for integration: (i) the active and floating gate poly are self-aligned together (ii) floating gate poly (F-poly) is patterned by CMP without photolithography, circumventing the possible misalignment problem. As shown in Fig. 1(b) SA-STI scheme is different from SAP in that a trench profile is made by STI etch using F-poly (FG1). Besides, for high capacitive coupling between control gate and floating gate, SA-STI scheme requires additional F-poly layer (FG2) and a photolithography to pattern F-poly. The F-poly photo process must be strictly controlled to avoid the misalignment between point A to point B in Fig. 1(b). The TEM images of the final structure are shown in Fig. 2.

Threshold Voltage Dispersion

The Vth measured from 512K cells after block erase is shown in Fig. 3. The erase Vth dispersion resulting from SAP is narrower than that of SA-STI. This can be understood in correlation with the difference in the edge profile of tunnel oxide. Figs. 4 and 5 show the simulated F-N tunneling currents for erase in SAP and SA-STI oxides, respectively. The majority of the F-N tunneling current is confined in the center of active area in SAP structure (Fig. 4), while significant portion of the current extends over edge of active area in SA-STI (Fig. 5). The high edge field in the latter should be sensitively affected by the variation of edge profile. We carried out additional simulations using various edge profiles in Figs. 6 and 7.

Fig. 6 shows the F-N current variation for different edge profiles in SA-STI. The variation of bird's beak oxide at the F-poly edge, "A to D" results in different current levels (Fig. 6(a)), while the different F-poly recess "a to e" gives rise to significant current fluctuation (Fig. 6(b)). The series of experiments performed during the course of this work has shown that the parameters of the bird's beak and F-poly recess are hard to control throughout the etch process of the trench and the oxidation process on the trench edge.

Fig. 7 shows the variation of F-N current versus edge profile in SAP. Here, the corner profile of F-poly edge, moving from "A to E"(see inset) rapidly reduces the tunneling current, effectively suppressing the current beyond the oxide thickness level, C for STI edge area.

Fig. 8 shows the simulation of the erase Vth. The larger Vth dispersion in SA-STI confirms the sensitive role played by the edge profile in SA-STI, compared to SAP. Here, the Vth's were first simulated for structures with chosen tunnel oxide(ΔT_{OX}) and edge profile (ΔE) variations, yielding a family of Vth vs. ΔT_{OX}, ΔE plots. Then, 10^6 samples of Gaussian random variations were generated and Vth's are calculated at each point by interpolating the prepared plots. Fig. 9 shows the Vth dispersion vs. the random variance $3\sigma_{TOX}$ or $3\sigma_E$ in SAP for different cell widths (W). As shown, the oxide random variance, $3\sigma_{TOX}$ is the major contributor to Vth broadening rather than the edge thickness, $3\sigma_E$. As the cell shrinks, the effect of $3\sigma_E$ grows exponentially, but still is much less than that of $3\sigma_{TOX}$, indicating the suitability of SAP for scaling.

The fluctuation in the F-N tunneling causes a large dispersion of erase Vth, and in turn generates over-erased cells having negative Vth which leads to a false data reading. Furthermore, about 40% of Vth window is taken by the erase Vth dispersion [3]. This means that SAP structure having narrower dispersion provides wider Vth window for MLC operation, compared with SA-STI.

Endurance Characteristic

Fig. 10 shows the endurance characteristics of the cell, where program and erase are done by channel hot electron injection and channel F-N tunneling, respectively. Clearly the SA-STI structure exhibits endurance disadvantages. The upward shift of its erase Vth after 500K cycles is larger than that of SAP by 0.5V. This could be attributed to, (i) the subsequent oxidation processes for curing damage on trench edge cannot restore the original oxide quality, and (ii) the oxide suffers from the severe degradation due to F-N tunneling in SA-STI edge [4-6].

Conclusion

We have shown that in addition to key process advantages for integration SAP process improves the cell performances, e.g. narrow erase Vth dispersion and superior reliability suitable for multilevel operation. We successfully fabricated 256Mb MLC NOR flash memory chip, using scalable SAP process. We have also demonstrated the well-defined multi-level Vth states satisfying the requirements such as wide Vth window, small erase Vth dispersion, highly reliable endurance and retention characteristics, as shown in Fig. 11.

References

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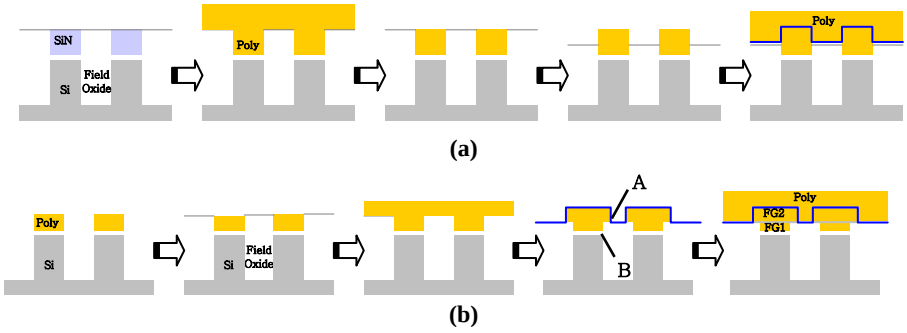

Fig. 1. Process sequence. (a) SAP (Self-Aligned Poly) Process (b) SA(Self-Aligned)-STI Process

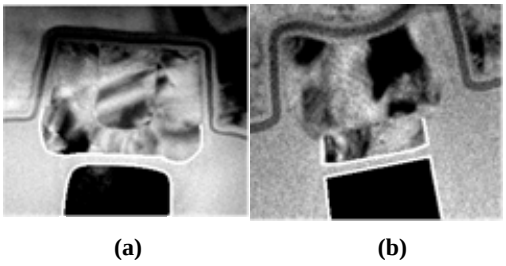

Fig. 2. TEM cross section of (a) SAP process cell and (b) SA-STI process cell

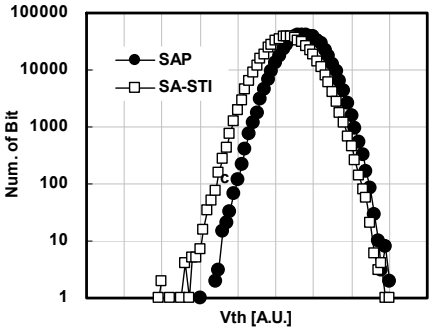

Fig. 3. Erase Vth dispersion

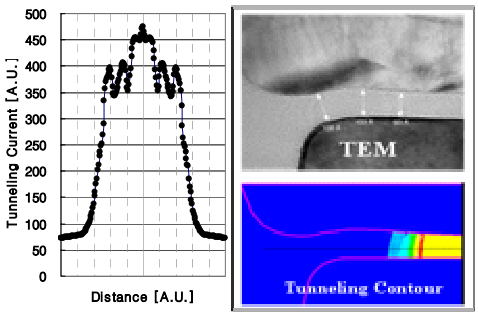

Fig. 4. SAP process active profile and F-N tunneling simulation for erase.

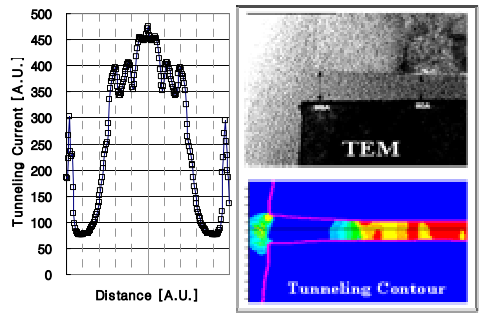

Fig. 5. SA-STI process active profile and F-N tunneling simulation result for erase.

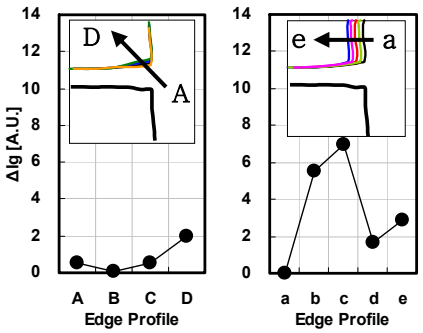

Fig. 6. Simulated F-N tunneling current in SA-STI process active profile.

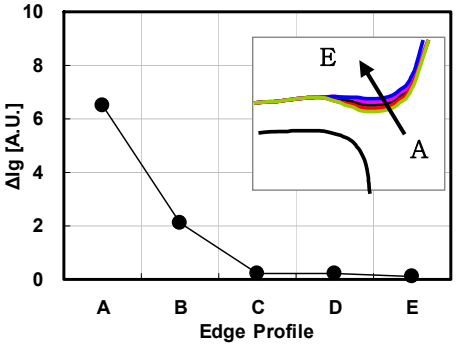

Fig. 7. Simulated F-N Tunneling current in SAP process active profile.

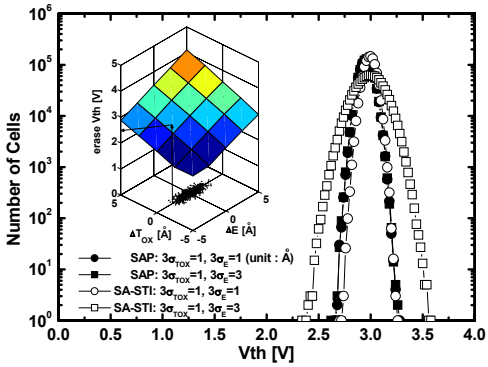

Fig. 8. Simulated erase Vth dispersion with process random variations ($3\sigma_{TOX}$ & $3\sigma_E$) in SAP and SA-STI

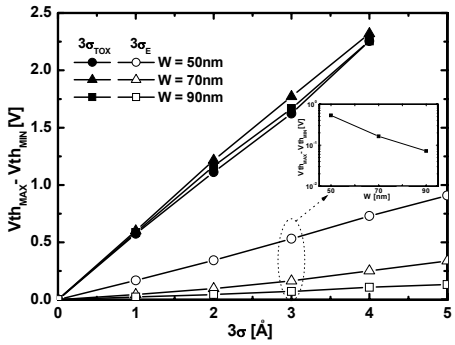

Fig. 9. Simulated Vth dispersion vs. process random variation for different cell widths in SAP

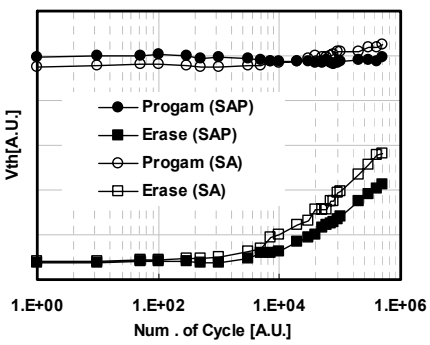

Fig. 10. Endurance characteristics of SAP and SA-STI process cells.

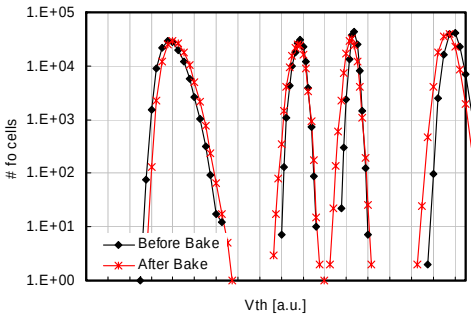

Fig. 11. Multi-level V_{th} distribution of SAP process cell. The retention characteristics before and after high temperature bake, 24 hours at 150° C after 10k cycling