Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.1026-1027

H-7-1 (Invited)

Current Development Status and Future Challenge of FeRAM Technologies

S.Y. Lee and Kinam Kim

Semiconductor R & D Center, Memory Division, Semiconductor Business, Samsung Electronics Co. Ltd.,
San #24, Nongseo-Ri, Kiheung-Eup, Yongin-Si, Kyungki-Do, Korea
Phone: +82-31-209-3603 Fax:+82-31-209-3274 E-mail: hjjoo@samsung.com

1. Introduction

FRAM having non-volatile and random access memory functions with extreme low power and high speed is the best candidate for next generation mobile memory [1]. In order for FRAM to be fully utilized in future mobile memory applications, the cell size of FRAM should be comparable to those of conventional mobile memories such as DRAM or NOR Flash. By the progresses in 1T1C, COB cell technologies, FRAM with 2-D stack capacitor cell structure, almost identical to that of DRAM at around 180~250 nm technology nodes have been successfully demonstrated [2,3]. But still there a wide gap in cell size exists between current FRAM and conventional mobile memories with cell size of 8~10F^2 beyond 100 nm technology node. Figure 1 shows sensing margin as a function of cell size at various technology nodes assuming that cell size is linearly scaled down with the current 2-D stack capacitor cell. As indicated here, as far as sensing window is concerned, current 2-D stack capacitor cell will be only extendable to the cell size around 12~15F^2 at 130 nm technology node. Beyond that, 3-D capacitor cell like current DRAM cell should be developed. In this paper, the most updated 2-D stack capacitor cell 1T1C FRAM technologies are discussed from which 12F^2 sized cell at 150 nm technology node has been successfully demonstrated. Furthermore, 3-D capacitor technologies which will be very useful for future FRAM with the cell sizes of 6~8F2 beyond 100 nm technology node are suggested.

2. 2-D stack capacitor technologies for 12F^2 cell at 150nm technology nodes

2-D stack capacitor will be effectively scaled down while keeping relatively large capacitor area if the space between capacitors could be patterned with the minimum pitch size in a given technology node and is illustrated in Fig. 2. In order to succeed in the patterning of minimum pitch spaced 2-D capacitors at nm scaled technology node, new capacitor etching technology for providing steep slope angle of an etched capacitor as well as new capacitor stack technologies for providing robust 2-D capacitor at reduced electrode and PZT thicknesses should be developed and is indicated in Fig. 3.

Under 200 nm thick capacitor stack technologies

Ferroelectric capacitors with IrO_2/Ir electrode and MOCVD PZT showed excellent retention and endurance characteristics compared to those with Pt electrode and sol-gel PZT [4]. But IrO_2/Ir-MOCVD PZT ferroelectric system is known to suffer from the ferroelectric degradation, especially in retention, as the thickness of PZT film scales down [5]. The origin of the degradation has been reasoned to be an interfacial non-ferroelectric layer and should be treated for the further scaling of PZT film [5]. We have developed a novel electrode technology against the degradation. Fig. 4 and 5 shows 2Pr and retention characteristics of MOCVD PZT film capacitor with new oxide electrode as a function of MOCVD PZT film thickness. By the application of new electrode, robustness of MOCVD PZT film is maintained on the PZT film as thin as 60 nm.

Steep slope one mask etching technologies

Former one mask etching technologies with TiN hard mask only provide 70^o etching slope on 300~350 nm thick capacitor stack. In order to improve etching slope, new multi-layer hard mask scheme where overall hardness of hard mask was reinforced by the compositional change of previous single mask layer and an addition of a second mask layer. Chemical environment was also modified for the best slope. Fig. 6 compares resulting capacitor patterns produced by former one mask etching technologies and new double mask etching technologies. It is clear that great improvement in etching slope was achieved by developing an advanced double mask capacitor etching technologies.

Performance of 1T1C FRAM with 12F^2 cell size at 150 nm technology node

Fig. 7 illustrates a cross-sectional SEM image of a unit cell of our experimental 150 nm/12F^2 cell 1T1C FRAM. Table 1 shows the device features of our experimental 0.27 um^2 sized cell 1T1C FRAM and Fig. 8 shows hysteresis of cell capacitors after full integration. By using new double mask etching technologies and novel oxide electrode capacitor stack technologies, FRAM cell is reduced to 0.27 um^2 in size, smallest cell size ever reported, where robust 200 nm thick 2-D stack capacitor is occupied with >50% capacitor to cell area ratio. Such large capacitor to cell ratio was achieved by the safe separation of 2-D stack capacitor spaced with 150 nm minimum pitch size with 77^o etching slope. The Degradations arising from the metal interconnection processes were prevented by the application of Al_2O_3 hydrogen barrier layers and by the proper choice of inter-metallic oxides. Fig. 9 shows the cell charge distribution of a 64k bit cell array and Fig. 10 shows the decay of sensing window as a function of bake time at 150^{o}C. No significant retention decay was found on 0.11 μm^2 sized cell capacitor with the new 2-D capacitor stack technologies.

3. 3-D stack cell technologies for 6~8F^2 cell beyond 100 nm technology node

Conformal and uniform deposition of electrode and ferroelectric material along the trench hole are the pre-requisite requirements for the success of 3-D ferroelectric capacitor for future FRAM. Fig. 11 shows TEM image of our earlier 3-D capacitor stack deposited on a trench hole patterned with 0.35 μm in diameter and 0.4 μm in depth. 20 nm thick Ir was deposited as a bottom electrode and 70 nm thick MOCVD PZT film was applied for a 3-D ferroelectric film. Fig. 12 shows the results of XPS composition analysis on a 3-D PZT film along the trench hole. As indicated in Fig. 11 and 12, the conformality of Ir bottom electrode was greatly improved by the application of new deposition method, atomic layer deposition. Compositional uniformity of MOCVD PZT along a trench hole was achieved by the introduction of a novel PZT chemical source. However, closer look at the TEM image revealed that granular PZT structure where abnormal pyrochlore phase PZT growth was made was found in the side wall portion of the 3-D PZT film. Thus preventing granular PZT defects in 3-D PZT is one among the key technical challenges for the perfect 3-D capacitor essential for 6~8F^2 cell FRAM beyond 100 nm technology node. We recently developed new MOCVD PZT deposition technology from which an excellent columnar PZT structure was grown on the most part of a trench hole and is shown in Fig. 13. As a result, for the first time in the world, robust ferroelectric hysteresis was obtained on 3-D PZT capacitor and is shown in Fig. 14. It can be concluded that the major challenges against 3-D capacitor are solved and a perfect 3-D capacitor for sub 10F^2 cell can be obtainable in the near future.

4. Conclusion

In order to succeed in developing high density FRAM, new 1T1C, COB integration technologies different from the conventional 2-D stack capacitor cell technologies should be developed. 1T1C FRAM technologies for 150 nm technology node such as steep slope capacitor etching technology and 200 nm thick capacitor stack technologies have been successfully developed and been demonstrated with an experimental 0.27 um^2 cell 1T1C FRAM. By newly developing 3-D capacitor stack technologies such as ALD Ir and new MOCVD PZT deposition method, robust ferroelectric hysteresis was measured on a preliminary 3-D capacitor for the first time. It can be concluded that the success in realizing 1T1C FRAM at 150 nm technology node and 3-D capacitors for 100 nm technology node can provide a great opportunity for FRAM to be utilized as a future mobile memory.

Reference

[1] Kinam Kim, plenary talk, 2004 ISIF, Gyeongju, Korea, 2004
[2] H.H. Kim *et al*., Symp. on VLSI Tech. Dig., P210, 2002
[3] J.H. Park *et al*., IEDM Tech. Dig., p594, 2004
[4] H.J. Joo *et al*., Symp. on VLSI Tech. Dig., P148, 2004
[5] Y.M. Kang *et al*., Symp. on VLSI Tech. Dig., P102, 2005

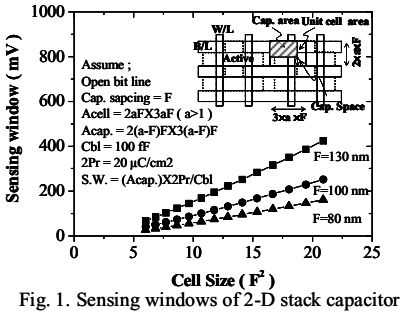

Fig. 1. Sensing windows of 2-D stack capacitor as a function of a cell size with various capacitor-to-cell ratios ; 200 mV of sensing window is assumed to be minimal for safe sensing of 1T1C FRAM.

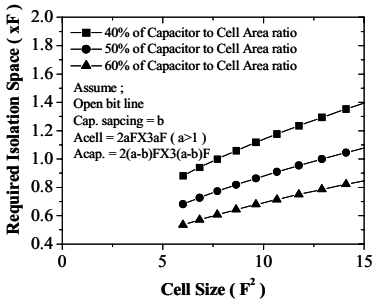

Fig. 2. Required minimum isolation space between capacitors as a function of a cell size at various capacitor-to-cell area ratios.

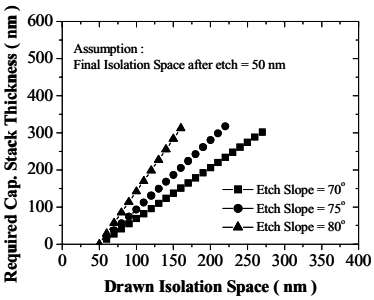

Fig. 3. Required thickness of capacitor stack for the safe separation of an isolation space between capacitors as a function of drawn isolation space at various etching slopes.

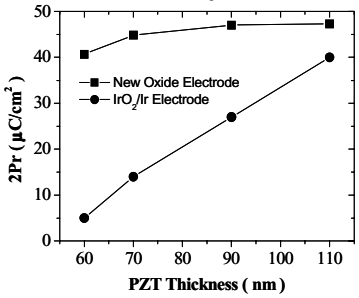

Fig. 4. 2Pr of MOCVD PZT capacitors with new oxide electrode as a function of PZT film thickness.

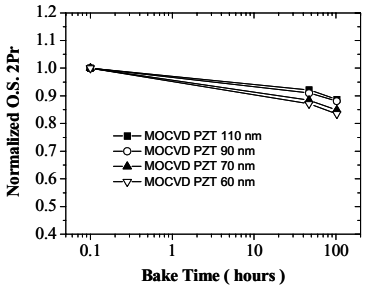

Fig. 5. 2Pr decay of MOCVD PZT capacitors at 150°C bake with new oxide electrode and various PZT film thicknesses.

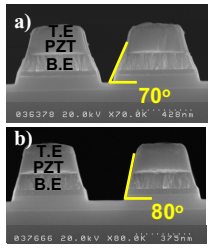

Fig. 6. SEM image of one-mask etched capacitors ; a) with previous etching, b) with new double mask etching.

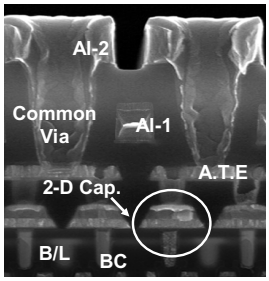

Fig. 7. A vertical SEM view of a unit cell of an experimental 0.27 μm² cell 1T1C FRAM after full integration.

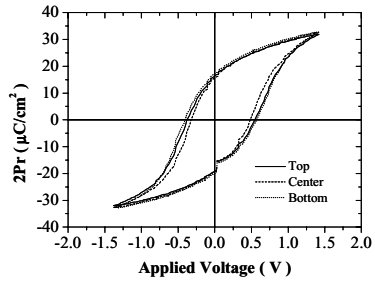

Fig. 8. Hysteresis of 0.11 μm² sized capacitor in a 0.27 μm² sized unit cell of an experimental 1T1C FRAM after full integration.

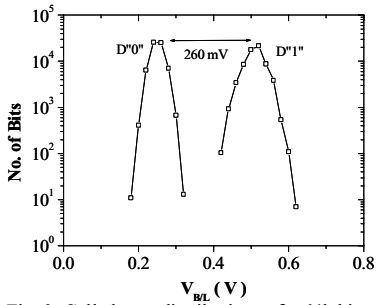

Fig. 9. Cell charge distributions of a 64k bit FRAM cell array of 0.27 μm² sized cell at 1.2V.

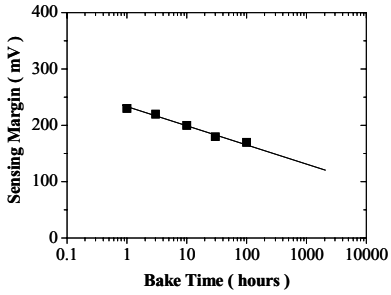

Fig. 10. Degradation of sensing window of a 64k bit FRAM cell block as a function of baking time at 150°C.

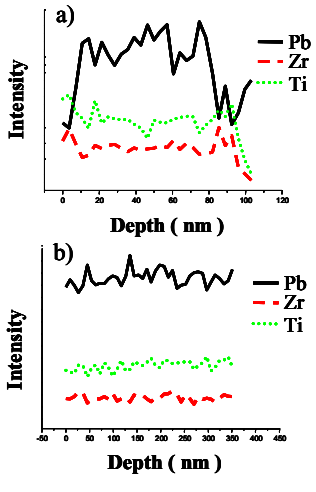

Fig. 12. XPS analysis results on the composition of 3-D PZT film along a trench hole ; a) top portion of trench hole, b) side wall portion of a trench hole.

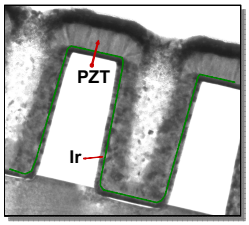

Fig. 11. A precision TEM image of a 3-D MOCVD PZT film and ALD Ir deposited in a trench hole with previous MOCVD PZT technologies.

Process Features	
Design Rule	0.15μm
Cell Size	0.27μm²
Cap. Size	0.11μm²
Interconnection	W Plug,
Metallization	4 Level Metal (W, Al1, Al2, Al3)
Cap. Stack	Ir/Buffer Electrode/ PZT/Ir/TiAlN, 200nm
Cap. Thickness	70nm

Table 1. Process features of 0.27 μm² sized 1T1C FRAM.

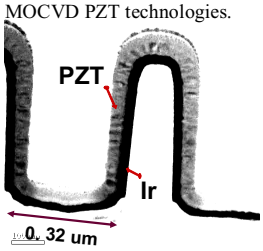

Fig. 13. A precision TEM image of a 3-D MOCVD PZT film and ALD Ir deposited in a trench hole with new MOCVD PZT technologies.

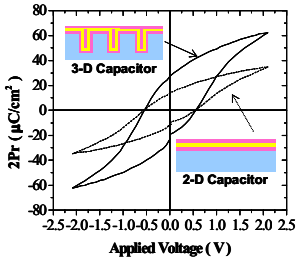

Fig. 14. Hysteresis of 3-D capacitor with new MOCVD PZT technologies.