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Highly Reliable 0.15μm/14F^2 Cell FRAM Capacitor using $SrRuO_3$ Buffer Layer

J.E. Heo, B.J.Bae, D.C.Yoo, S.D.Nam, J.E.Lim, D.H.Im, S.O.Park, H.S.Kim, U.I.Chung and J.T.Moon

Process Development Team, Semiconductor R&D Division, Samsung Electronics Co. Ltd.,
San #24, Nongseo-Ri, Kiheung-Eup, Yongin-Si, Kyungki-Do, Korea
Phone: +82-31-209-3665 Fax:+82-31-209-2729 E-mail: james.heo@samsung.com

1. Introduction

Recently, the development of PZT films has reached a stage where it can be considered a leading candidate for ferroelectric random access memories (FRAM) [1]. Achievements such as the large remnant polarization, low coercive voltage and low crystallization temperature have placed PZT films in promising candidate. In our previous papers, we proposed a 1 transistor 1 capacitor cell structure with 0.25 μm design rule, 15F^2 cell size for stand alone FRAM device [2]. For high density 64Mbit and beyond FRAM devices, a reduction in capacitor stack height is essential [3]. However, there are many issues that still need to be improved to extend the limit to storage density. In order to achieve successful shrinkage of the device, the PZT capacitor must be formed as a thin stack. As thin PZT capacitors tend to show more severe problems to retention and fatigue caused by degradation between conductive metal oxide and PZT film [4], it is also necessary to address these problems. In this report, we have developed a highly reliable PZT capacitor realizing 0.15μm design rule, 14F^2 cell size for 1.4V operation. Recent investigations have shown that this is only possible when PZT film scaled below 80nm [5]. We therefore used 75nm thick-PZT with an overall thickness of 180nm for the whole capacitor stack. In particular, we will describe the interfacial degradation phenomenon between conductive metal oxide and PZT film using $SrRuO_3$ buffer layer.

2. Characteristic of highly reliable 0.15μm/14F^2 cell capacitor

As in our previously reported devices, for our highly reliable 0.15μm /14F^2 cell PZT capacitors we have used W/TiN plug as bottom contact and Ir/TiAlN layers sequentially stacked on the plug as bottom electrode. $Pb(Zr_xTi_{1-x})O_3$ (PZT) grown by metal-organic chemical vapor deposition (MOCVD) was used as ferroelectric layer. The capacitor patterning was performed by a one-step mask etching scheme with a TiAlN mask. In the following properties of the patterned capacitors will be discussed. It is well known that scaling down PZT film thickness results in a degradation of polarization due to the increase of the interface portion. This can be seen in Fig. 1, where it is shown that the thickness dependent degradation results in a 2Pr value of only 10μC/cm^2 for 75nm thickness. It has become well known that the degradation of thin PZT capacitors is caused by interfacial microstructure defects. In order to reduce these interfacial defects we inserted a top $SrRuO_3$ buffer layer using DC magnetron sputtering. $SrRuO_3$ has the same perovskite structure as PZT and shows good lattice matching at the top interface as shown in Fig. 2. The effect of $SrRuO_3$ on remnant polarization is shown in Fig. 1. It can be seen that the 2Pr value is greatly enhanced if $SrRuO_3$ is used for the top electrode. The remnant polarization of the 75 nm thick-PZT with $SrRuO_3$ buffer layer is above 40μC/cm^2, which is a great enhancement compared to PZT without buffer layer. This result is obviously due to the lower interfacial defect density as discussed above. Applying $SrRuO_3$ also at the bottom electrode results in similar 2Pr values as for top electrode alone. These results indicate that to improve ferroelectric characteristics of PZT capacitors the interface should be modified to decrease defects. Fig. 3 shows the remnant polarization as a function of voltage of 75nm thick-PZT capacitor with top and bottom $SrRuO_3$ buffer layer. The remnant polarization of saturation voltage reaches around 1.2 V to show 40μC/cm^2. Hysteresis loops of the as grown PZT film capacitors are as shown in Fig. 4. As expected, the symmetric capacitor stack with $SrRuO_3$ buffer layers at the top and bottom electrode tends to be superior in process-induced imprint behavior compared with inserting only at the top interface of the PZT layer.

Next the reliability properties for capacitors with $SrRuO_3$ applied at the top and bottom electrode will be discussed. For investigation of retention properties we performed baking tests at 150 ^{o}C. Time-dependent behavior of the polarization is shown in Fig.5. After baking for 100hrs less than 15% loss of opposite state remnant polarization is observed. Fatigue properties are shown in Fig. 6. No fatigue degradation is seen up to 1E11 switching cycles at 1.4V.

3. Integration technologies for high density FRAM device with thin capacitor stack

An additional issue that arises as a result of the overall reduction of capacitor stack height is the reduction of the bottom Ir barrier to less than 40 nm. Negative effects are the out-diffusion of oxygen from the PZT layer resulting in oxidization of the W plug. Moreover, out-diffusion of Pb results in reaction of Pb with SiO_2. These effects result in defects as shown in Fig. 7 a) and b), respectively. In order to prevent those effects, an enhancement of the bottom barrier layer is needed. In Fig. 7 c) it can be seen, that using a $SrRuO_3$ buffer layer is very effective in improving the reactive defects mentioned above. This means that the $SrRuO_3$ buffer layer plays an important role as a Pb and O blocking layer between PZT and bottom electrode. Fig. 8 shows cross-sectional vertical-SEM image of additional top electrode (ATE). Fig. 9 and Fig. 10 show a comparison of remnant polarization as a function of applied voltage and hysteresis loops at the AS-CAP and ATE integration level for capacitors with $SrRuO_3$ buffer layer. It can be concluded that the use of $SrRuO_3$ buffer layer considerably enhances ferroelectric characteristics of PZT capacitors and enables the realization of 180nm capacitor stacks with 75nm thick-PZT.

4. Conclusions

We developed highly reliable 0.15μm design rule/14F^2 cell capacitors with 75nm-thick PZT for FRAM devices with 1.4V operation voltage. Using $SrRuO_3$ buffer layers inserted at the top and bottom interface of the PZT layer dramatically enhanced ferroelectric characteristics. These competitive results meet the requirements for high density 64Mbit and beyond FRAM device.

References

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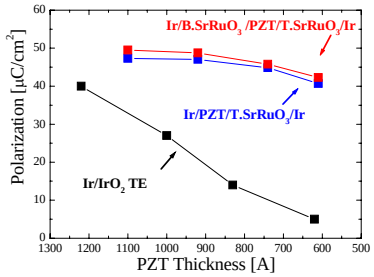


Fig. 1 Remnant polarization as a function of PZT thickness with different electrodes Ir/PZT/Ir capacitor.

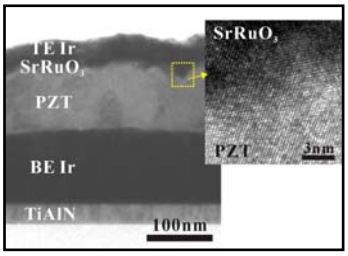


Fig. 2 Bright-field and high-resolution TEM micrographs showing the interfacial atomic structure between $SrRuO_3$ and PZT films.

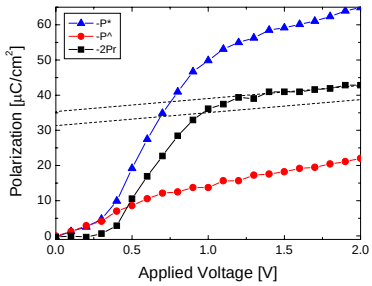


Fig. 3 Remnant polarization as a function of applied voltage of 75nm thick-PZT capacitor.

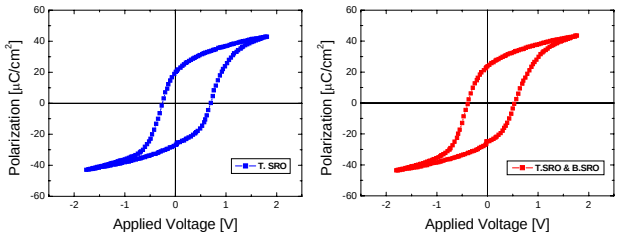


Fig. 4 Comparison of P-V hysteresis loops of PZT capacitor using (a) top buffer $SrRuO_3$ and (b) top and bottom buffer $SrRuO_3$ between PZT interface after retention test.

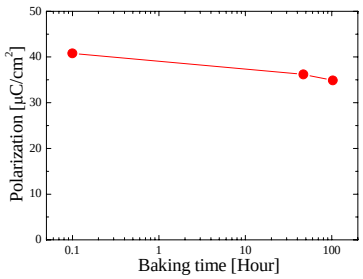


Fig. 5 Opposite-state polarization margin of 75nm PZT capacitor as a function of storage time after retention test at 150 °C.

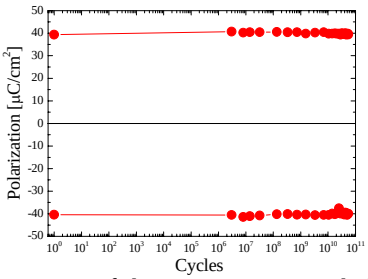
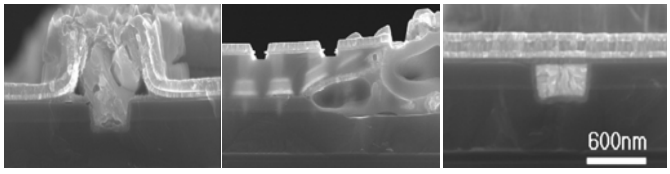


Fig. 6 Fatigue property of the PZT capacitor with $SrRuO_3$ buffer layer at 85 °C.



(a) (b) (c)

Fig. 7 SEM cross sections of samples (a), (b) without $SrRuO_3$ buffer layer and (c) with $SrRuO_3$ buffer layer in 75nm thick-PZT.

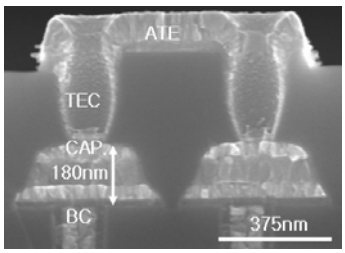


Fig. 8 Cross-sectional vertical-SEM image of ATE -0.15μm /14F^2 cells.

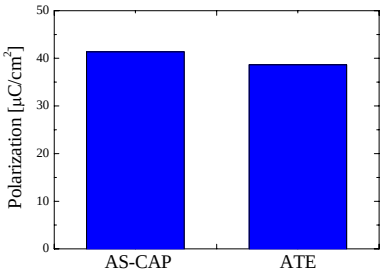


Fig. 9 Comparison of remnant polarization at AS-CAP and ATE integration proceeds.

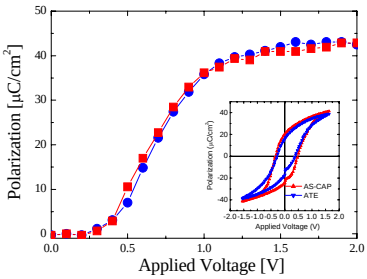


Fig. 10 Remnant polarization as a function of applied voltage and hysteresis loops of 75nm PZT capacitor with $SrRuO_3$ buffer layer.