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Bit Distribution and Reliability of High Density 1.5V FRAM Embedded with 130nm, 5LM Copper CMOS Logic

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Abstract

High density FRAM, operable at 1.5V, has been fabricated within a 130nm, 5LM Cu/FSG logic process. To evaluate FRAM extendability to future process nodes, we have measured the bit distribution and reliability properties of arrays with varying individual capacitor areas ranging from $0.40\mu m^2$ (130nm node) to $0.15\mu m^2$ (~65nm node). Wide signal margins, stable retention (>>10yrs at 85ºC), and high endurance read/write cycling (>>10^{12} cycles) have been demonstrated, suggesting that reliable, high density FRAM can be realized.

1. Introduction

Ferroelectric memories (FRAM) are the most promising alternative to traditional embedded non-volatile (NV) memories, such as flash and EEPROM, because of their fast read/write cycle time, NV data retention, low voltage/low power operation and low number of additional masks for fabrication [1]. Intense efforts are underway to commercialize this technology [2]. In this work, we demonstrate for the first time excellent bit distribution characteristics and reliability properties obtained on these aggressively area-scaled high-density arrays operating at 1.5V. The arrays feature capacitors with on-silicon capacitor areas down to $0.15\mu m^2$. By using standard single-gate oxide and 5LM Cu/FSG interconnect processes, we demonstrate that the FRAM module is fully compatible with advanced CMOS processes, and portable between various logic families.

2. Device and Process Features

Table I describes key embedded FRAM design features at the 130nm logic node with projections to the 65nm node. Cap areas ranging from 0.40 to $0.15\mu m^2$ are investigated to identify any potential issues with FRAM planar scaling. Both cap area and bitline capacitance are reduced with each successive node to maintain signal margin. Beyond 65nm, we anticipate that 3-D structures will be required. The FRAM module, formed between the Contact and Metal 1 levels of a standard logic flow, is shown in the cross-sectional SEM micrograph (Fig. 1). The ferroelectric capacitor stack is composed of a TiAlN bottom electrode diffusion barrier, Ir bottom electrode, MOCVD $Pb(Zr_{0.25}Ti_{0.75})O_3$ ferroelectric film, Ir/IrO_x top electrode and TiAlN hard mask [1]. The cap stack in Fig. 1 is defined through a single-mask and etched using a multi-sequence RIE process. AlO_x serves as the hydrogen diffusion barrier; SiN_x as an etch stop layer; and SiO_2 is the planarized ILD. A second mask defines the bi-level vias that connect Metal 1 to either the top of the ferro-capacitor or to Contact. All process modifications to mitigate hydrogen-induced degradation to the caps are confined to the FRAM module. Previous work has shown that the FRAM module has negligible impact on the CMOS electrical properties [1].

3. Array Characteristics

Figure 2 shows the bit distribution histogram for a 144kb segment (~700kb/mm^2 macro density) of $0.40\mu m^2$ area capacitors. The distributions are well formed and separated with good signal margin. Note that the signal level is normalized to take into account the load capacitance (~480fF) and capacitor area. The opposite state distribution for 64kb arrays (Fig. 3), baked at 150°C for up to 1000hrs, indicates that the OSR0 (Opposite State Read 0) is stable; OSR1 degradation is only about 20% for 1000hrs bake, suggesting >>10yr lifetime at 85ºC. Fig. 4 corroborates minimal OS degradation (approx. 11% after 1000hrs bake at 150°C for the 16kb array); no additional weak bits were identified. An accelerated fatigue mode on the test chip permits rapid testing of 8,192 bits [3]. Bit distribution measurements at 1.5V through 10^{12} cycles using this mode (Fig. 5) are marked by stable Data 0; a "wake-up" phenomenon occurs with Data 1, leading to an increase of the signal margin even after 10^{12} read/write cycles.

The bit distributions of 0.40 and $0.15\mu m^2$ cap arrays, expressed in switched polarization, are shown in Fig. 6. The peak in P_{sw} is similar for both cap sizes, with a wider distribution for the smaller cap. Endurance measurements for the $0.15\mu m^2$ cap arrays (Fig. 7) cycled up to 10^{13} cycles exhibit remarkable similarity to that of the $0.40\mu m^2$ cap arrays (Fig. 5) described earlier. In Fig. 8, the %OS margin remaining (normalized difference between average OS1 and OS0) measured on the packaged $0.15\mu m^2$ cap arrays is plotted as a function of bake time at different temperatures – the gentle slope of the straight lines is noteworthy. At 6000 hrs, 125°C bake, up to 70% of signal margin is retained.

In summary, we have demonstrated 1.5V operation of an FRAM memory integrated into a standard 130nm CMOS process with 5LM Cu BEOL. Bit distributions of highly scaled cap arrays varying from 0.40 to $0.15\mu m^2$ show wide signal margin, endurance exceeding 10^{13} cycles, and high signal margin retention.

References

[1] T. Moise et. al., IEDM Tech. Dig. (2002) 535.
[2] H. J. Joo et al., Symp.VLSI Tech Dig. (2004) 148.
[3] J. Rodriguez et al., IEEE TDMR. **4** (2004) 436.

Table I FRAM road map shown for different nodes. Product values are listed for 130nm node; estimates for other nodes.

Production Node (nm)	**130**	**90**	**65**
Metal 1 half-pitch (nm)	175	135	90
Supply Voltage (V)	1.5	1.2	1.1
Cell type	2d	2d	2d
Mask Adder	2	2	2
Cell Area (μm^2)	0.71	0.35	0.24
Cap Area-Silicon (μm^2)	0.36	0.18	0.13
Bitline Capacitance (fF)	240	180	120

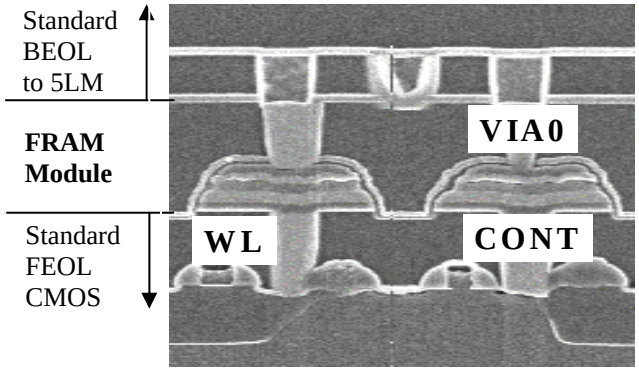

Fig. 1 Cross-sectional scanning electron micrograph illustrating placement of the FRAM module betwixt CONT and MET1 levels.

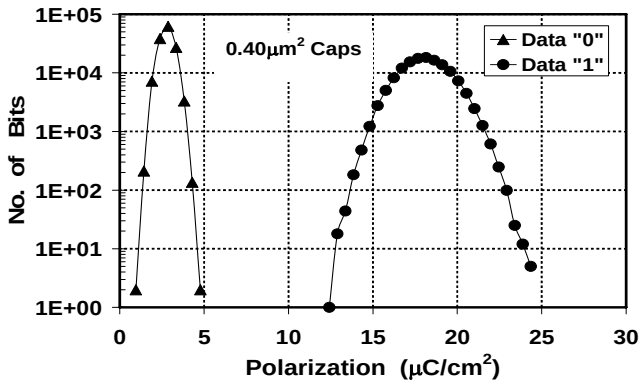

Fig. 2 Bit distribution histogram taken at 1.5V for 144kb segment. Good separation and sense margin are evident.

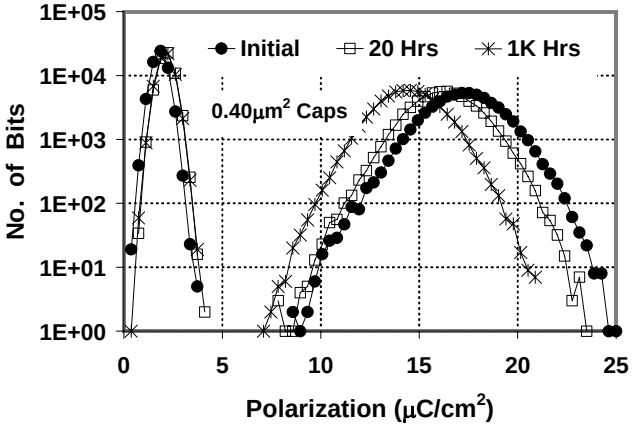

Fig. 3 Opposite State bit distribution plotted as a function of cumulative bake time. Opposite State Read 1 controls the magnitude of signal margin remaining.

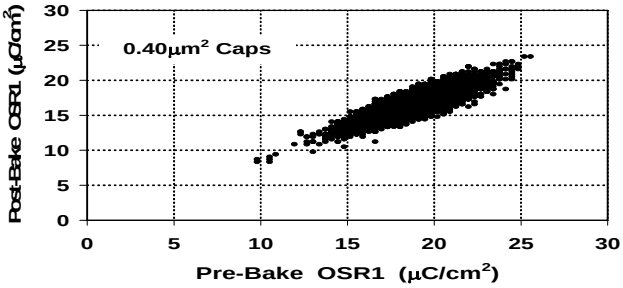

Fig. 4 Plot of post-bake OSR1 (150°C for 1000hrs) against pre-bake OSR1, expressed in polarization, for 0.40μm^2 caps.

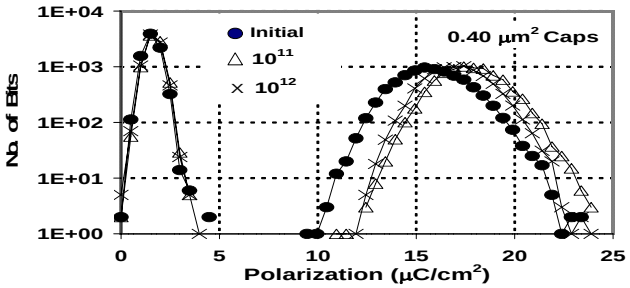

Fig. 5 Bit distribution measurements through 10^{12} cycles at 1.5V.

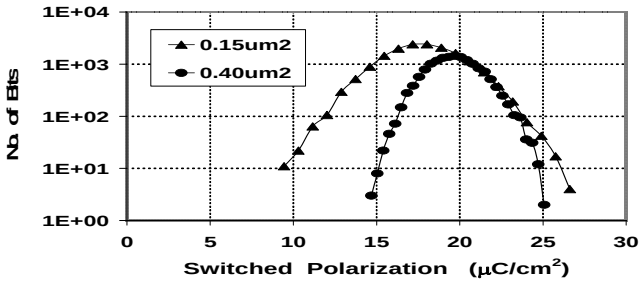

Fig. 6 Bit distribution histogram taken at 1.5V for two cap sizes.

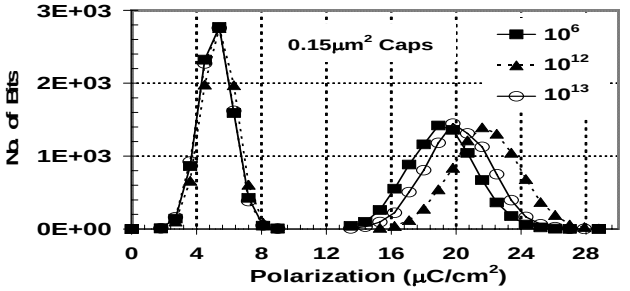

Fig. 7 Bit distribution measurements through 10^{13} cycles at 1.5V.

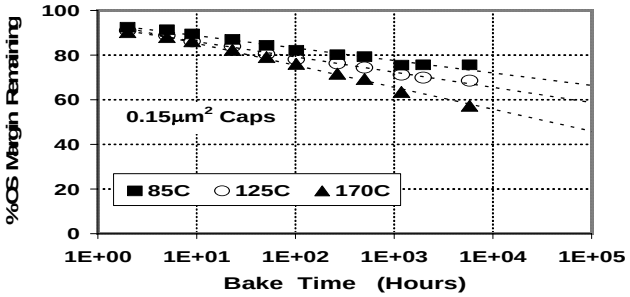

Fig. 8 Opposite state margin remaining plotted against bake temperature and time for packaged 0.15μm^2 memory cap arrays.