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Multi-bit Programming for 1T-FeRAM by Local Polarization Method

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1. Introduction

FeRAM has such distinctive features as nonvolatality, low power consumption. FeRAMs are being mass-produced up to the capacity of 1Mbit. However, FeRAM applications are limited at present because of restriction of the memory capacity. MFIS-FET which has ferroelectric layer between gate and insulator, is a 1-transistor type memory device and has minimal cell size. In this study, multi-bit programming performed on MFIS-FET for the further increase of the capacity of FeRAM.

2. Experiment

MFIS-FET

MFIS-FET was fabricated as shown in fig. 1. Ferroelectric layer and insulator layer were formed using (Bi, Nd)$_4$Ti$_3$O$_{12}$ (BNT) which has appropriate coercive field and HfO$_2$ [1][2][3] which has excellent channel characteristics, respectively.

Data programming method

Data programming method for multi-bit memory is shown in fig. 2. For "Write 1" and "Write 2", pulses of +8V or -8V were applied to gate while drain, source, and body were held at ground level, corresponding to typical writing method for "on" state and "off" state. Pulse width was 10ms for all write operation. "Write 3" pulse was applied after "Write 2" operation to switch the polarization of the ferroelectric on the channel area. A pulse of –8V was applied to gate, drain and source, while body was held at ground level. Similarly, "Write 4" pulse was applied after "Write 1" to switch the polarization on the source area. A pulse of +8V was applied to gate, drain and body, while source was kept at ground level.

Read process is shown in figure 3. The gate voltage was held at a voltage between –0.4V and +0.4V, and drain voltage was held at –0.1V.

3. Result and discussion

Figure 4 shows the change of read out current after each write operation. The current level for "Write 3" and "Write 4" were between those for "Write 1" and "Write 2" which are conventional "on" and "off" state. Comparison of the polarization states for "Write 2" and "Write 3" or "Write 1" and "Write 4" reveals that the polarization on the drain region has dominant influence on the current level.

Figure 5 shows the results of read out current with different gate voltage. The four write states are able to be distinguished by the shift of the threshold voltage. The signal margin might be optimized by the device parameter such as channel length or ferroelectric properties. Moreover, 3bit programming can be achieved by source-drain exchange at write and read operation.

4. Conclusions

Multi-bit programming was performed on MFIS-FET. The polarization of the ferroelectric on the channel and source / drain region was controlled locally by the combination of programming bias, which resulted in the change of the read out current in four levels. The result showed the possibility of further increase of capacity of FeRAM.

References

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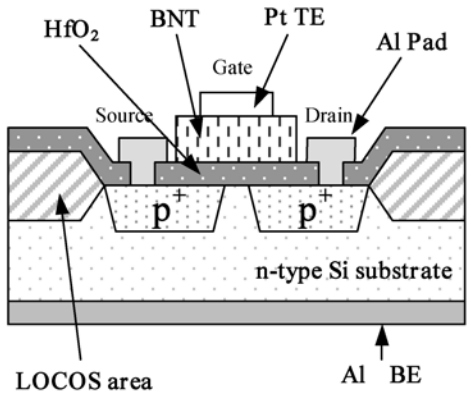

Fig. 1 A cross section of the fabricated MFIS-FET

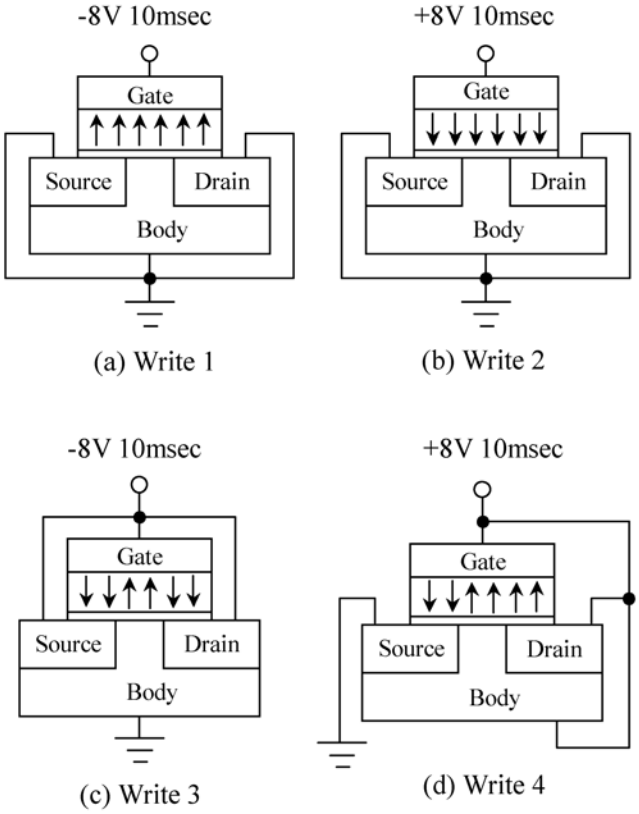

Fig. 2 Write method

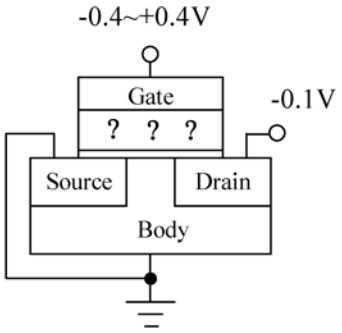

Fig. 3 Read method

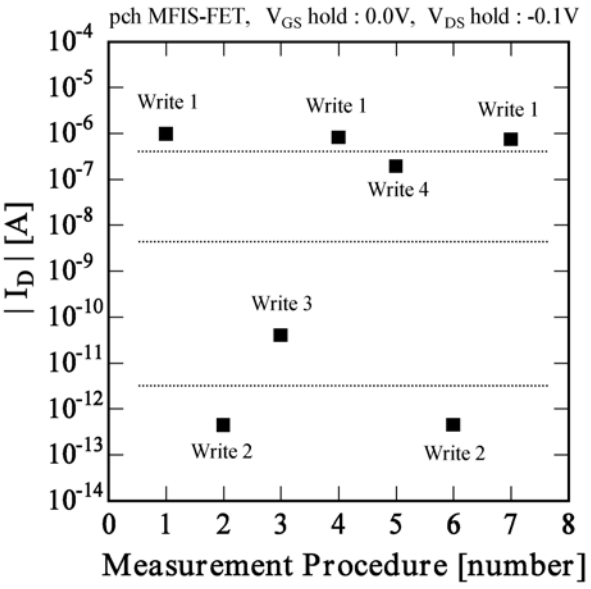

Fig. 4 Read out current after various write operation. The gate voltage is 0V.

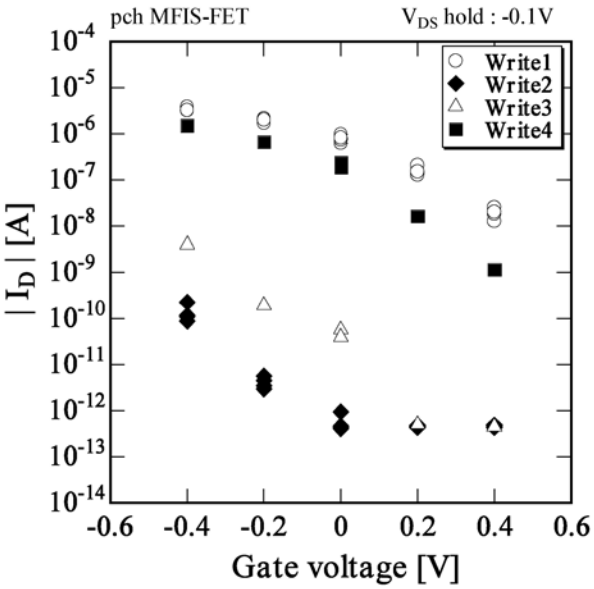

Fig. 5 Relation between read out current and gate voltage for each write state.