Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.1040-1041

H-9-1 (Invited)

Overview and Future Challenges of MRAM Technologies

S. Tehrani, B.N. Engel, J.M. Slaughter, M. Durlam, N. Rizzo, R. Dave,
J. Sun, J. Janesky, S. Pietambaram, and F. Mancoff

Freescale Semiconductor, Inc.
1300 N. Alma School Road, Chandler AZ 85224 - USA

1. Introduction

Magnetoresistive random access memory (MRAM) employs a magnetoresistive device integrated with standard silicon-based microelectronics, resulting in a combination of qualities not found in other memory technologies. For example, MRAM is non-volatile, has unlimited read and write endurance, and has demonstrated high-speed read and write operations. We present here an overview of the characteristics and future challenges of MRAM based on Magnetic Tunnel Junction (MTJ) devices, with emphasis on recent developments in 4Mb Toggle-MRAM devices.

2. Overview of MRAM Technology Status

The development of MRAM technology has faced many challenges impacting the manufacturability of high-density devices. One of the main hurdles has been to achieve adequate write switching and disturb margins to support reliable 10-year operation. The "conventional" Stoner-Wolfarth bit select and writing approach described in the literature to date [1] has not been able to achieve the necessary operating margin. Toggle-MRAM, with its unique bit material stack and switching method has emerged as an approach that achieves sufficient write and read margins to support manufacturable, competitive devices. The Toggle-MRAM bit cell uses a balanced synthetic-antiferromagnetic free layer and a phased-pulse write sequence (see Fig. 1) for programming. The unique properties of this switching approach virtually eliminate the half-select disturb mechanisms that have posed a significant challenge to the manufacturability of conventional MRAM.

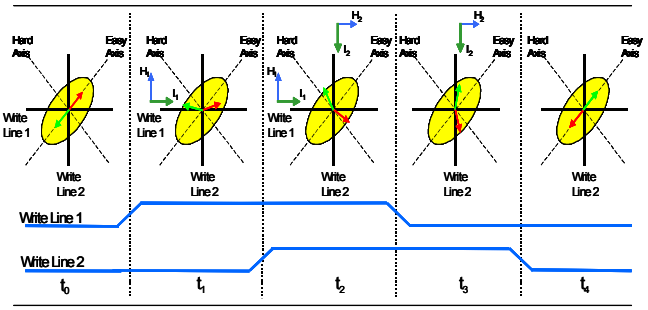

Fig. 1 Program operation of Toggle-MRAM switching. Pulses are applied in a sequence designed to rotate the bit Free-Layer 180 degrees to the opposite resistance state.

MRAM Reliability

The Toggle-MRAM switching method has enabled successful sample introduction of 4Mb MRAM devices into the marketplace. MRAM introduces a number of new materials and materials interfaces not encountered in standard CMOS technology where endurance and reliability are crucial requirements. Recent data from full 4Mb MRAM arrays displays good reliability over 10 years against dielectric breakdown, resistance drift, programming current drift, electromigration, and with solid data retention.[2]

Tunnel Barrier Reliability

Time-dependent dielectric breakdown (TDDB) is detected as an abrupt increase of junction current due to a short forming through the tunneling barrier. The increase in current is accompanied by a loss of essentially all the MR. From a memory circuit perspective, a shorted junction results in a stuck-at-zero bit failure. Statistically significant data were obtained using a custom designed 1kb memory reliability circuit processed simultaneously with the 4Mb arrays. The 1kb memory array is designed to allow for accurate measurements of the applied bias stress over the bit as well as the bit resistance during stress. The circuit has voltage measurement points just above and below the MTJ to allow for an accurate measurement and control of the MTJ stress bias at all times. Fig.2 shows typical TDDB data obtained from the 1kb reliability array.

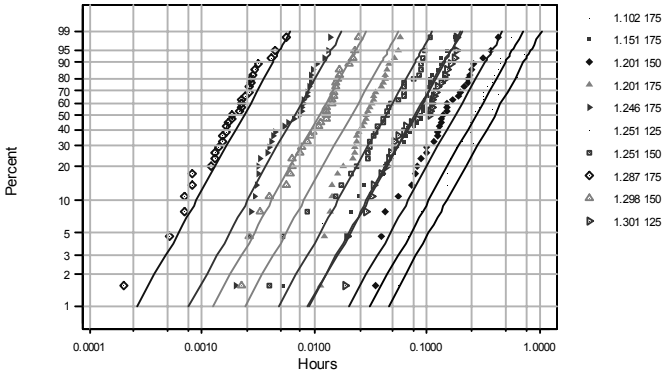

Fig. 2 TDDB data from 1K reliability arrays.

The data can be well fitted (straight lines) by a model based on Weibull life-time distributions, linear-E bias acceleration and an Arrhenius type thermal activation. The strong bias acceleration and the relatively low operating bias (typically 0.3V) predicts several orders of magnitude more intrinsic reliability than required for 10 years operation, even for the worst case usage of continuous addressing of one word. This high level of reliability against dielectric breakdown was confirmed in full 4Mb arrays.

Data Retention

The information stored in the free layer of the MTJ has two stable states separated by a single energy. The timescale on which MRAM is therefore non-volatile is determined by the size of the energy barrier, E, separating these states relative to thermal energy, kT. For 10 years the

barrier must be at least 70 kT. Accelerated testing was carried out on 532 4Mb parts at elevated temperatures (up to 240C). The test consists of writing a checkerboard pattern into the memory, applying the temperature for a given time and reading the memory for state reversals. Under all conditions, we observed NO state changes due to thermal agitation. Theoretical analysis of thermal activation (Fig. 3) indicates that the nonvolatility of the 4Mb parts is therefore better than required for 1 FIT (1 PPM in 10 years).

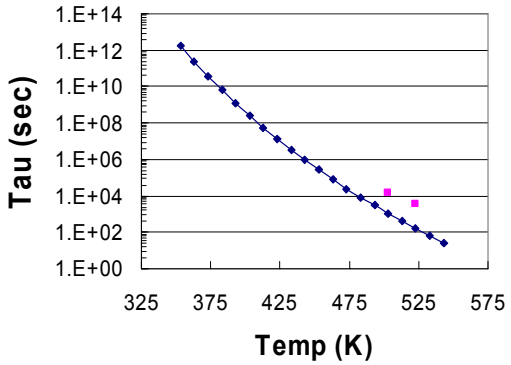

Fig. 3 Diamonds are the theoretical curve of the time required to observe 1 state change in 532 4Mb parts versus measurement temperature with E/kT = 70. The squares are measured data for time with NO observed state changes in 532 4Mb parts at two temperatures, exceeding the requirement for 1 FIT nonvolatility at operating temperature (1 PPM in 10 years).

***Read Speed Improvements – MgO Tunnel** Barriers*

The high TMR values obtainable with MgO-based magnetic tunnel junctions (MTJs) could enable significant performance improvements in MRAM. One issue limiting the introduction of MgO barriers is that the ferromagnetic materials (CoFeB) that have been used to obtain TMR>200% do not have the magnetic properties needed for good switching. However, MgO barriers used with NiFe-based Toggle freelayers display significantly higher TMR ratios than provided by AlOx junctions. Figure 4 is a plot of TMR obtained from NiFe SAF freelayers compatible with

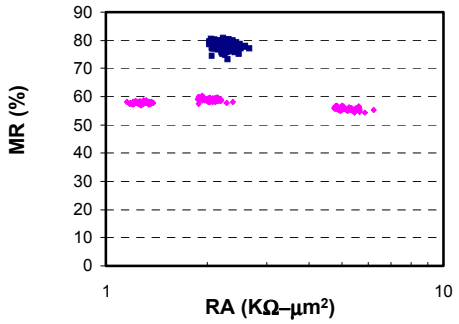

Fig. 4 Enhanced TMR from NiFe-based Toggle freelayers with MgO barriers.

Toggle MRAM, showing ~2x improvement over conventional AlOx. Continued improvements of the magnetic properties of CoFeB-based materials show great promise for MRAM with TMR ratios near 200%.

Write Current Reduction

There has been a great deal of research in the field on lowering the MRAM write current further to achieve lower power and higher density. For example, a new multilayer Toggle free-layer employing four antiferromagnetically coupled ferromagnetic layers was recently proposed and demonstrated by Toshiba-NEC. [3] By using a strong coupling layer to couple two weaker SAF structures, it was shown that the Toggling field could be lowered by nearly 2x over the single SAF Toggle stack, without reducing the operating window from saturation.

We presently are investigating a novel approach to lowering the write current that focuses on improving the current-to-magnetic field conversion efficiency of the write lines. We have found that the magnetic field B produced at the bit can be increased by enhancing the permeability, μ of the surrounding dielectric material. We have made enhanced permeability films by embedding superparamagnetic nanoparticles in a dielectric matrix. We have found with a μ ~ 5, Hsw was reduced by up to 45%. This is a very promising approach to improve the write power of MRAM.

As MRAM is scaled to smaller dimensions, there is a possibility to use the Spin Momentum Transfer (SMT) effect to switch the bit state by passing current directly through the bit. SMT is the interaction between a ferromagnet and a spin-polarized current flowing through it, causing at net torque on the ferromagnet that can cause state reversal. The current density required for this switching is relatively high (~10^6 A/cm^2), but at small enough bit geometries, the current itself can be small. We have been investigating using SMT in low RA tunnel junction bits for MRAM switching . In Fig. 5 are representative plots of SMT switching in MgO tunnel junction bits sized ~ 80 nm x 160 nm and ~150 nm x 290 nm, showing switching currents < 1 mA. With suitable architecture changes and process improvements, SMT is a promising candidate for low power, high density MRAM at advanced CMOS nodes.

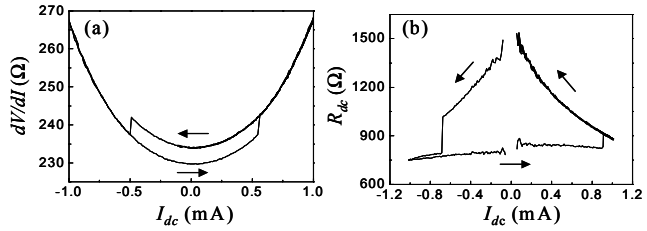

Figure 5: (a) Measured differential resistance *dV/dI* vs. I_{dc} for an MTJ bit of low *RA* (~2.3 Ω-μm^2) and *TMR* (~2%). (b) Measured dc resistance Rdc vs. I_{dc} for an MTJ bit of higher *RA* (~27 Ω-μm^2) and *TMR* (~79%).

[1] S. Tehrani et al., IEEE Proceedings, Vol. 91, No. 5, May 2003, pp. 703-714.

[2] J. Åkerman et al., Proc. 43rd IEEE Int. Symp. Reliability Physics, pp. 163-7, 2005

[3] T. Suzuki et al., 2005 Symp. VLSI Technology Digest, pp. 188-9