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New Magnetic Flash Memory with FePt Magnetic Floating Gate

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1. Introduction

Demand for a high density and high performance non-volatile memory has rapidly grown as the global market for mobile information devices has expanded in ubiquitous society [1]. Various kinds of non-volatile memories have been proposed and investigated. Flash memory is the most widely used non-volatile memory because it has several advantages such as high density, low manufacturing cost, stable operation and so on. In recent years, however, flash memories face a serious problem concerned with a trade-off between reliability of charge retention and scaling down of oxide film thickness. Besides, it also has problems of drain turn-on effect and floating gate capacitive coupling between adjacent cells [2]. In order to solve these problems, we proposed a new non-volatile memory with FePt magnetic floating gate which is called "Magnetic Flash memory". In this study, we investigate the fundamental characteristics and electrical properties for this new Magnetic Flash memory.

2. Basic Structure of Magnetic Flash memory

Figure 1 schematically shows a cross sectional structure of a memory cell for Magnetic Flash memory. As is obvious in the figure, one-transistor type memory cell is used in the Magnetic Flash memory. The magnetic FePt film inserted between the blocking oxide and the magnetic control gate acts as a floating gate. Furthermore, FePt magnetic film, tunneling oxide and magnetic control gate compose a magnetic tunneling junction (MTJ). The NiFe magnetic control gate acts as a free layer and the FePt magnetic film acts as a pinned layer in this MTJ. The tunneling probability between the free layer and the pinned layer depends on the relative magnetic polarization of them, parallel or anti-parallel. The tunneling probability is high in the case of the parallel polarization for both free layer and pinned layer and low in the case of the anti-parallel polarization for them. The parallel polarization is preserved in the programming mode and the erasing mode whereas the anti-parallel polarization is preserved in the retention mode. The switching magnetic field to change the magnetic polarization between the parallel and the anti-parallel is produced by both currents flowing through a bit line (BL) and a word line (WL). Furthermore, a positive high voltage or 0V is applied to the control gate depending upon the programming data "1" or "0", respectively, in the programming mode. The control gate is maintained at the ground potential. Therefore, electrons are injected from the control gate into the floating gate when the data "1" is written. Meanwhile, in the erasing mode, a positive voltage is applied to the control gate through the word line preserving the source and the drain at the ground potential in order to emit electrons in the floating gate to the control gate. Thus, excellent retention characteristics are expected even if the thinner tunneling oxide is used because the MTJ is in the anti-parallel polarization condition. Consequently, a higher programming and erasing speed can be achieved in this new Magnetic Flash memory with the magnetic floating gate maintaining the advantage of capability for scaling-down the memory cell size.

3. Results and Discussion

Figure 2 shows the magnetization characteristics of FePt thin film which is used as a floating gate and magnetic pinned layer. The FePt thin films with the thickness of 100nm were formed by RF-sputtering on the thermally grown silicon oxide and annealed at different temperatures using the rapid thermal annealing (RTA) method. The crystallographic structure of FePt film transformed from fcc to the $L1_0$ phase. Clear hysteresis loops are observed in Fig.2. In addition. large coercivities were obtained after annealed at 400ºC. Therefore, it was confirmed that the FePt film can be used as the magnetic pinned layer which should have the large coercivity. Figure 3 shows the X-ray diffraction patterns of the double layers of SiO_2(10nm)/ FePt(100nm) annealed at various temperatures for 10min. With increasing annealing temperature from 200ºC to 650ºC, the fct (111) peak of FePt becomes stronger, indicating the enhanced FePt chemical ordering. Above 400ºC, two-phases of Fe_2O_3 and FePt ordered alloys mixed. These results indicate that the oxidation of Fe occurs by RTA at 400ºC and higher temperature. We used a reactive ion etching (RIE) to form the FePt floating gate pattern with small size although it is known that the RIE of FePt is difficult. Figure 4 is the SEM cross-sectional image of FePt floating gate formed by RIE (ECR) with CO/ NH_3 mixed gas. The etching rates was 14nm/min. The tantalum film with the thickness of 10nm was used as a hard mask for etching. It is obvious from Fig.4 that FePt floating gate with small size is successfully formed by RIE (ECR) with optimized etching conditions. Figure 5 is the magnetization characteristics of MTJ with structure of FePt (20nm)/ SiO_2 (3nm)/ NiFe (20nm). The FePt films are annealed at 300ºC for 10min by RTA. Clear hysteresis curve is obtained in Fig.5. The switching magnetic fields of NiFe (20nm) and FePt (20nm) were 0.021kOe and 1.6kOe, respectively. Thus, Fig.5 demonstrates that the FePt thin film can act as a pinned layer and NiFe can act as a free layer. Fundamental electrical characteristics of the Magnetic Flash memory were evaluated using MOS capacitor and MTJ. Figure 6 shows the C-V characteristics of MOS capacitor with FePt floating gate (20nm) and NiFe control gate. The area size of capacitor gate is 1.5㎛×6㎛. Many capacitors with such small gate area were connected to obtain a larger capacitance value. The total

capacitor gate area is 100μm×100μm. The MTJ consists of FePt (20nm)/ SiO_2 (3nm)/ NiFe (20nm). As is clear in the figure, large hysteresis loops were observed in the C-V characteristics showing the flat band voltage shift of 1.8V. The hysteresis caused by the charging and discharging of electrons in the FePt floating gate appears in the C-V curves. The charging and discharging of electrons occur between the FePt floating gate and the NiFe control gate. Negative voltage is applied to the NiFe control gate in order to inject the electrons from the NiFe control gate into the FePt floating gate. As is clear in Fig. 6, the flat band voltage shift was changed by the polarity of magnetic polarization after applying the magnetic field. Figure 7 shows the I-V characteristics of MTJ with FePt pinned layer (20nm) and NiFe free layer. As is clear in the figure. the tunneling current for the parallel magnetic polarization was larger than that for the anti-parallel polarization.

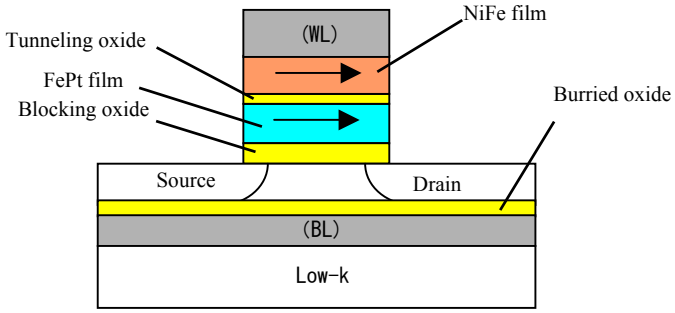

Figure 1 Cross-sectional view of the new magnetic flash memory with FePt magnetic floating gate.

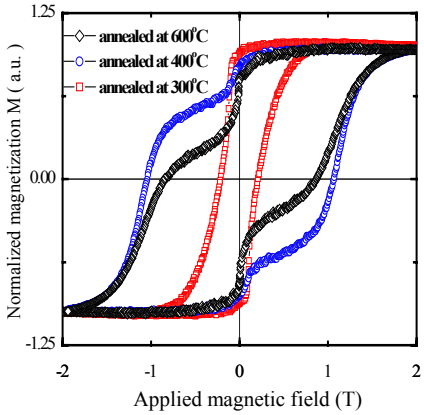

Figure 2 Magnetization characteristics of FePt thin films (thickness: 100nm) annealed at different RTA temperatures.

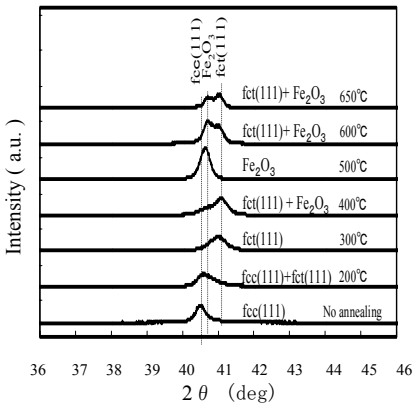

Figure 3 XRD patterns of FePt thin film (thickness: 100nm) as a function of annealing temperatures.

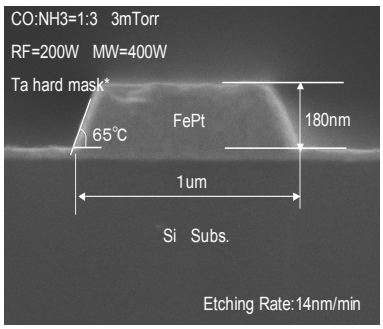

Figure 4 SEM image of FePt magnetic floating gate formed by reactive ion etching with CO/ NH_3 mixed gas.

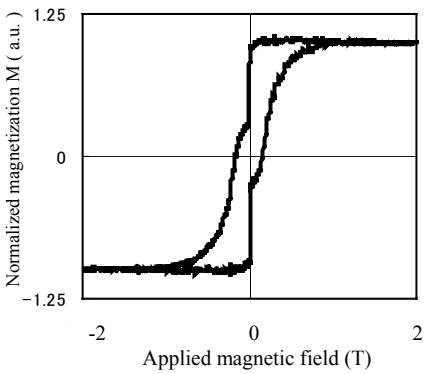

Figure 5 Magnetization characteristic of MTJ with structure of FePt (20nm)/ SiO_2 (3nm)/ NiFe (20nm).

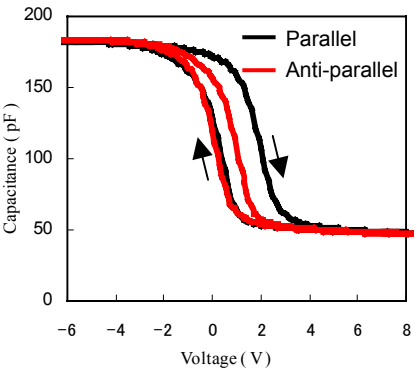

Figure 6 C-V characteristics of MOS capacitor with FePt floating gate (20nm) and NiFe control gate.

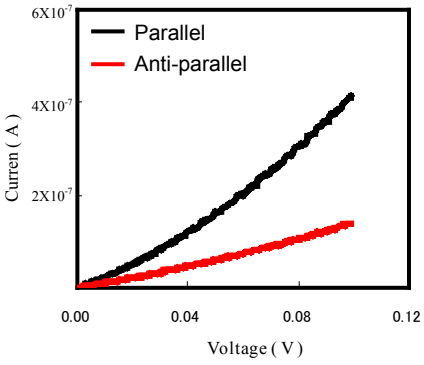

Figure 7 I-V characteristics of magnetic tunneling Junction (MTJ) with FePt pinned layer (20nm) and NiFe free layer.

Both C-V and I-V characteristics indicated that the magnetic tunneling effect occurs between the FePt floating gate and the NiFe control gate. Thus, the fundamental memory operation of Magnetic Flash memory was confirmed.

4. Conclusions

We proposed a new non-volatile memory with FePt magnetic floating gates called a Magnetic Flash memory. The switching magnetic fields of 0.021kOe for NiFe film and 1.6kOe for FePt film measured in MTJ with structure of FePt (20nm)/ SiO_2 (3nm)/ NiFe (20nm) indicated that the FePt thin film can act as a pinned layer and NiFe can act as a free layer. Fundamental electrical characteristics of the Magnetic Flash memory were confirmed using MOS capacitor and MTJ.

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