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High-Voltage 4H-SiC RESURF MOSFETs Processed by Oxide Deposition and N_2O Annealing

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1. Introduction

Silicon carbide (SiC) is a promising wide bandgap semiconductor for high-voltage power device applications, owing to the high critical electric field. Although prototype high-voltage SiC devices have been demonstrated based on recent progress in growth and device processing technologies, the performance of lateral SiC MOSFETs, more suited for future power IC applications, has still suffered from high on-resistance and relatively low breakdown voltage. Recent XPS and SIMS analyses have revealed that the SiO_2/SiC interface is not abrupt and a high density of carbon (SiC_xO_y or SiO_2+C) is detected near the interface [1]. Since the residual carbon near the interface might be inherent to thermal oxidation of SiC, the authors have investigated the potential of deposited oxides for SiC MOSFETs in this study. High-voltage SiC RESURF (reduced surface field) MOSFETs with a record performance are fabricated.

2. Improvement of MOS interface

SiO_2 films with a thickness of 80 nm were deposited on 4H-SiC{0001} epilayers by plasma CVD at 400°C. In order to improve the oxide quality, the samples were annealed in Ar or N_2O (10% in N_2) at 1300°C for 60-360 min. During the N_2O annealing (nitridation), the oxide thickness increased by Δd, as shown in Fig.1. MOS structures formed by "N_2O oxidation" at 1300°C [2] were also prepared as a reference.

Fig.2 depicts the current density–electric field characteristics of n-type 4H-SiC(0001) MOS capacitors formed by (i) plasma CVD and Ar annealing, (ii) plasma CVD and N_2O annealing, and (iii) N_2O oxidation. The typical characteristics among 20 MOS capacitors for each process are shown. Although the oxide formed by the "CVD+Ar anneal" process is leaky, N_2O annealing resulted in significantly improved dielectric properties (ρ = 10^{16} Ωcm, E_B > 10 MV/cm). Fig.3 represents the distribution of interface state density (D_{it}) for various MOS structures, which was determined from quasi-static and high-frequency *C*-*V* curves of n-type 4H-SiC(0001) MOS capacitors. The D_{it} values of "CVD+N_2O anneal" sample are lower near the conduction band edge (D_{it} = $3x10^{11}$ $cm^{-2}eV^{-1}$ @ E_C – 0.2 eV), compared to N_2O oxidation.

Inversion-type test MOSFETs were processed on p-type 4H-SiC{0001} epilayers. The MOSFET with a "CVD+Ar anneal" oxide showed a poor mobility of 4 cm^2/Vs, as predicted from its high D_{it}. Fig.4 plots the channel mobility against the increase of oxide thickness during N_2O annealing (Δd shown in Fig.1). At the Δd value of 5 nm, a maximum channel mobility of 34 cm^2/Vs was attained, being about 50% improvement compared to the standard N_2O oxidation. MOSFETs fabricated on the 4H-SiC(000-1) face showed an even higher mobility of 48 cm^2/Vs. SIMS measurements revealed the abrupt SiO_2/SiC interface and high nitrogen concentration at the interface ([N] = $8x10^{20}$ cm^{-3}) for "CVD+N_2O anneal" MOS structures.

3. Simulation and fabrication of RESURF MOSFETs

Fig.5 illustrates the schematic structure of a RESURF MOSFET fabricated in this study. Both the RESURF and LDD regions were 10 μm long and 0.6 μm deep. By the introduction of the LDD region, the optimum window in structure designing is widened [3]. RESURF MOSFETs were fabricated on 10 μm-thick p-type 8° off-axis 4H-SiC(0001) epilayers doped to $7x10^{15}$ cm^{-3}. The RESURF/LDD regions were formed by N^+ implantation, while high-dose ($4x10^{15}$ cm^{-2}) P^+ implantation was employed to form source/drain. The p^+ contact region was formed by Al^+ implantation. Post-implantation annealing was performed at 1700°C for 20 min in Ar with a carbon cap to suppress surface roughening. After RCA cleaning, the "CVD+N_2O anneal" process with the optimum condition (Δd = 5 nm) was applied to form the gate oxides. The contact metal was Ti/Al annealed at 600°C for source/drain and Al for gate. The typical channel length and width were 2 μm and 200 μm, respectively. The RESURF and LDD doses were optimized to reduce the electric field crowding at the drain edge and in the gate oxide by using device simulation (ISE-DESSIS).

Fig.6 plots the LDD-dose dependencies of experimental (average) and simulated breakdown voltages of 4H-SiC MOSFETs with a fixed RESURF dose of $2.4x10^{12}$ cm^{-2}. The simulated breakdown voltage is sensitive to the LDD dose, showing a maximum at a LDD dose of about $8x10^{12}$ cm^{-2}. At this LDD dose, the fabricated MOSFET also exhibited a maximum breakdown voltage as shown in Fig.6. In the simulation, the avalanching point is located at the drain edge in the case of a low LDD dose, and at the RESURF/LDD interface for a high LDD dose. The RESURF-dose dependencies will be discussed at the conference.

As shown in Fig.7, the best 4H-SiC(0001) MOSFET exhibited a high breakdown voltage of 1450 V with stable avalanche (without destructive failure) and a low on-resistance of 75 mΩcm^2 (μ_{eff} = 31 cm^2/Vs). The

threshold voltage was 3.6 V. These characteristics are better than those of the MOSFET with a N_2O-grown oxide and the same dose (1320 V – 84 mΩcm^2), and the present result is the best performance (V_B^2/R_{on} = 28 MW/cm^2) among any normally-off lateral MOSFETs (Fig.8).

4. Conclusions

Although the deposited oxides have not been an attractive choice in Si technology, the "CVD+N_2O annealing" is a promising process for SiC MOS devices. Using this technology, a 1450 V – 75 mΩcm^2 SiC RESURF MOSFET has been demonstrated.

[1] T. Kimoto et al.: Jpn. J. Appl. Phys. 44 (2005), 1213.

[2] L.A. Lipkin et al.: Mat. Sci. Forum **389-393** (2002), 985.

[3] T. Kimoto et al.: IEEE Trans. Electron Device **52** (2005), 112.

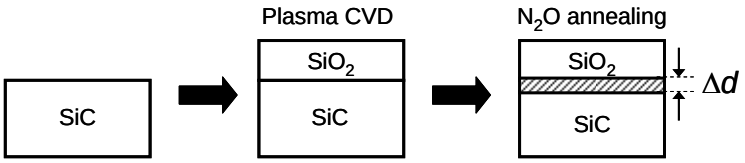

Fig.1 Schematic flow of "CVD + N_2O annealing" process. The increase of oxide thickness by N_2O annealing is denoted by Δ*d*.

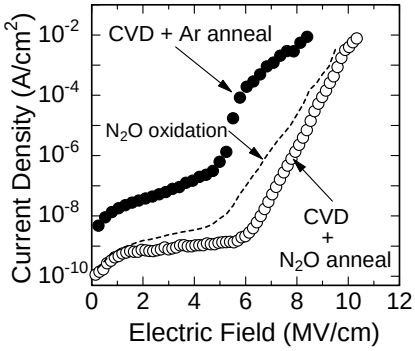

Fig.2 Typical current density – electric field characteristics of n-type 4H-SiC(0001) MOS capacitors formed by different processes.

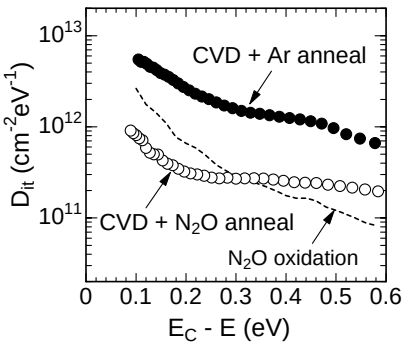

Fig.3 D_{it} distribution for n-type 4H-SiC (0001) MOS capacitors formed by different processes (determined by a hi-lo method).

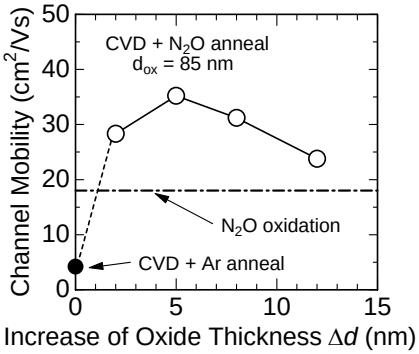

Fig.4 Effective channel mobility vs. increase of oxide thickness during N_2O annealing (4H-SiC(0001) face).

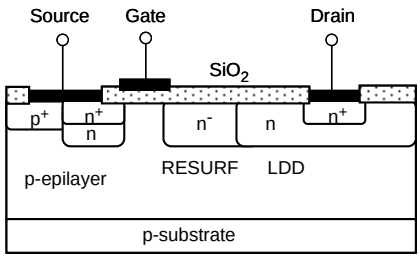

Fig.5 Schematic illustration of 4H-SiC RESURF MOSFET fabricated in this study.

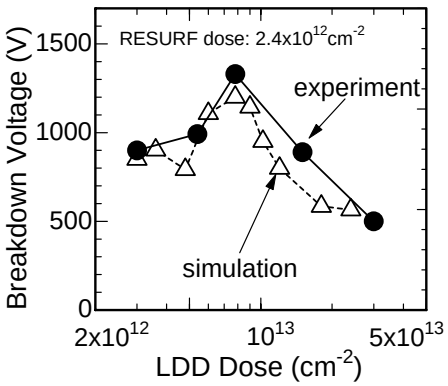

Fig. 6 LDD-dose dependencies of experimental and simulated breakdown voltages of 4H-SiC MOSFETs with a fixed RESURF dose of 2.4x 10^{12} cm^{-2}.

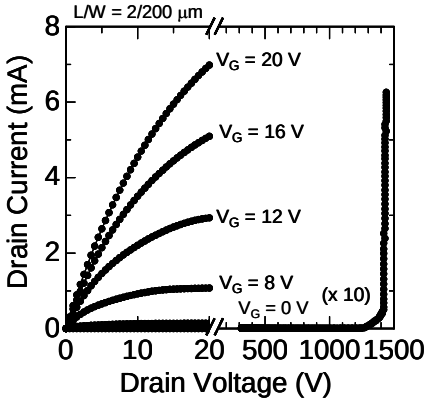

Fig.7 Drain characteristics of a 4H-SiC(0001) RESURF MOSFET with a deposited oxide followed by N_2O annealing at 1300°C.

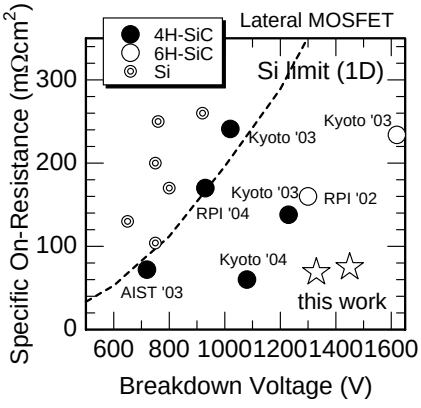

Fig.8 R_{on} vs. V_B for major lateral SiC and Si MOSFETs reported in literature and this work.