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Novel Differential-Mode RTD/HBT MOBILE-based D-Flip Flop IC

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1. Introduction

Recently, several leading research groups have demonstrated very high-speed operation near to 100 Gbps in master-slave D-type flip flops (MS D-FFs) with a source-coupled FET logic (SCFL) or an emitter-coupled logic (ECL) architecture [1], [2], [3], [4]. Typically, those high-speed results have been obtained at relatively high power dissipation of several-hundreds milli-watts or more. In order to realize more power efficient systems, the development of D-type flip flops (D-FFs), which operate at low DC power as well as at high speed, is crucial. Previously, the research on new D-FF topology based on negative differential resistance (NDR) digital ICs, using resonant tunneling diodes (RTDs), have shown its potential for high speed and low power operation from the inherent switching speed and reduced device count [5], [6]. The RTD-based D-FFs were implemented by utilizing monostable-bistable transition logic elements (MOBILEs) in a return-to-zero (RZ) mode using a MOBILE core only and a non-return-to-zero (NRZ) mode using a composite design of the MOBILE core plus a set/reset (SR) latch [6] ,[7]. Although these ICs sufficiently reduce the device count, their operation is based on the single-mode. However, in order to enable the MOBILE-based D-FF to be fully compatible with the conventional high-speed SCFL or ECL D-FFs, both dual-input and dual-output are required based on the differential-mode operation. Recently, a current-mode logic (CML)-type MOBILE-based D-FF has been successfully demonstrated in a NRZ mode for high speed operation, but its high-speed operation and full compatibility with the conventional high-speed SCFL or ECL D-FFs have not been realized [8], [9].

In this work, we propose and demonstrate a dual-input/output CML-type MOBILE-based D-flip flop with a new CML-type SR latch operating in a NRZ mode using an InP-based RTD/HBT IC technology. The proposed D-FF is based on the CML-topology in both MOBILE core and SR-latch, which solves the problem of unavoidable saturation-mode operation of the conventional SR latch. Therefore, the D-FF has its potential for high speed operation and full compatibility with the conventional ECL architecture at low static power operation compared to the conventional MS D-FF due to the sufficiently reduced device count.

2. Circuit configuration

The proposed D-FF is composed of a CML-type MOBILE core and a CML-type SR latch as shown in Fig. 1. In the MOBILE NRZ D-FF using the conventional SR-latch, which is composed of the cacaded pairs of RTD and HBT (or HEMT), the overall speed of the D-FF is limited by the lower operation speed of the SR-latch because of the HBT operation in the saturation region [7], [9]. To overcome this problem, a CML-type SR-latch is used in this work. Fig. 1 shows overall circuit configuration of the MOBILE-based NRZ D-FF. The basic operating principle of the CML-type MOBILE core is explained elsewhere [8], [9]. At the rising edge of the clock pulse, the state transition occurs. In this manner, it generates the complementary RZ-mode output signals. Fig. 2 shows the schematic of operating principle of the CML-type SR-latch. Since the outputs of the MOBILE core are in a RZ-mode, both outputs of it are always low, when V_{CLK} is low. In this case, the output of the SR-latch is at state "2" (or state "4"). Then, at the rising edge of V_{CLK}, the data voltage (V_{IN1}) of HIGH makes the output state of transistor Q_2 unchanged. This situation results in SET=LOW and RESET=HIGH. Therefore, the transition from state "2" to state "3" occurs and the OUT signal of the SR-latch changes to a HIGH state. Thereafter, when V_{CLK} is low, both SET and RETSET are low. Then, OUT remains a HIGH state. In this manner, the complementary outputs are successfully generated at the SR-latch output nodes according to the complementary input data in a rising edge-triggered NRZ-mode. The proposed D-FF has the advantages of about 1/3 reduction of device count over the conventional MS D-FF for the core circuit. In addition, it has the advantages of full compatibility to

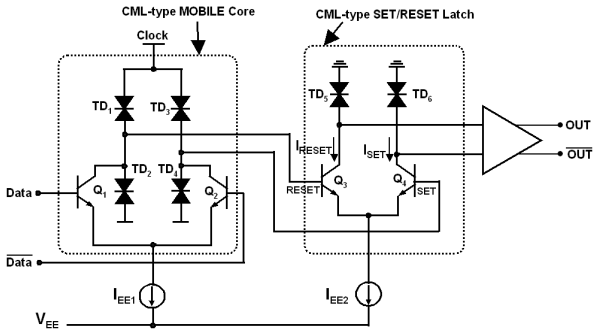


Fig. 1. Circuit configuration of the RTD/HBT MOBILE-based NRZ D-flip flop.

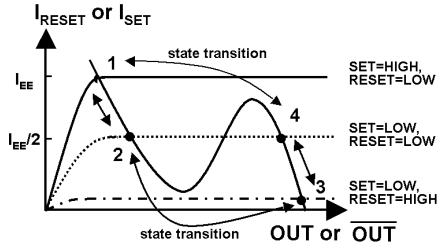


Fig. 2. Operating principle of the CML-type SET/RESET latch.

the conventional NRZ differential operation mode of the D-FF system architecture. Therefore, The proposed D-FF has its full potential for inherent high-speed and low-power operation.

3. Device structure and fabrication

The epitaxial layers were grown by MBE, and the devices were fabricated by using the optical lithography and wet etching technique. The details on the epitaxial layers and fabrication process are described elsewhere [8], [9]. The emitter size of the driver RTD and the load RTD were chosen to be 2×2 μm^2 and 2×4 μm^2, respectively. The peak current density (J_P) of the fabricated RTD was 80 kA/cm^2 with a good peak-to-valley current ratio (PVCR) of 12 at room temperature. The peak voltage of the device was 0.28 V. The HBT showed a current gain of 50 with a turn-on voltage of 0.75 V. The maximum f_T and f_{max} of the fabricated HBT with an emitter size of 2×5 μm^2 were 123 GHz and 82 GHz, respectively.

Fig. 3. shows a chip microphotograph of the fabricated CML-type MOBILE IC of which chip size is 0.5×0.5 mm^2.

4. Measurement results

In order to characterize the operation of the fabricated MOBILE IC at high speeds, a pulse pattern generator (Anritsu-MP1763B) was used to obtain the data stream and clock. The outputs of the fabricated IC were fed into a digital communication analyzer (Agilent 83484A). Fig. 4(a) shows a NRZ patterned bit stream (11011000) fed into the IC input at 12.5 Gb/s, which is the speed limit of the used test setup. The measured non-inverted (upper) and inverted (lower) output waveforms for the input data pattern of 11011000 are shown in Fig. 4(b). Fig. 5 shows the measured eye diagram for the operation with the input of a 2^{31}-1 psuedo-random bit stream. As shown in Fig. 4 and Fig. 5, the logic function of the fabricated MOBILE-based NRZ D-flip flop IC has been confirmed up to 12.5 Gb/s, which is the speed limit of the measurement setup. From the simulation results, the RTD/HBT D-FF is expected to operate up to over 30 Gbps. The measured DC power dissipation of the circuit was 45 mW at 12.5 Gb/s which is significantly low compared to the previous results having a similar emitter feature size of about 2μm [3], [4].

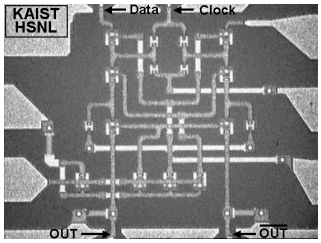
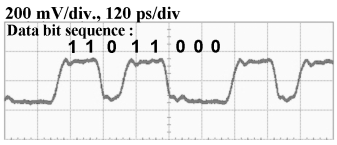
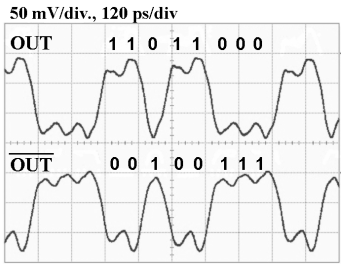


Fig. 3. Chip microphotograph of the fabricated MOBILE-based NRZ D-flip flop.



(a)



(b)

Fig. 4. (a) Input data stream and (b) non-inverted (upper) and inverted (lower) output waveforms of the fabricated MOBILE-based NRZ D-flip flop at 12.5 Gb/s operation.

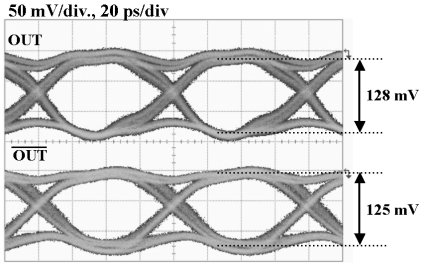


Fig. 5. Measured eye diagram for non-inverted (upper) and inverted (lower) outputs of the fabricated MOBILE-based NRZ D-flip flop at 12.5 Gb/s operation.

5. Conclusion

A novel RTD/HBT MOBILE-based NRZ D-flip flop IC with dual input/output has been successfully demonstrated and its speed performance has been confirmed up to 12.5 Gb/s. From the obtained clear eye opening and simulation results based on the measured device characteristics, the proposed D-FF is expected to operate up to over 30 Gbps. The results indicate that the proposed MOBILE-based D-FF has its potential for very high speed and low-power operation due to about 1/3 reduction of core device count as well as full compatibility with the conventional high-speed SCFL or ECL D-FF architecture.

Acknowledgements

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