Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.224-225

I-2-5

High-Speed Digital Circuits Using RTD as Load-Element

Hyungtae Kim, Sungjin Yeon, Sangsub Song, Sangho Park, Kwangseok Seo

Seoul National Univ., School Of Electrical Engineering and Computer Science
San 56-1, Shillim-dong, Kwanak-ku, Seoul 151-744, Korea
Phone: +82-2-877-0298 E-mail: kht086@snu.ac.kr

1. Introduction

In recent years, Resonant Tunneling Diodes (RTDs) technology is widely studied because they can achieve high-speed operation and high functionality with reduced circuit complexity and low power consumption owing to their Negative Differential Resistance (NDR) features. After Monostable-Bistable Transition Logic Element (MOBILE) was proposed ([1]), the monolithic integration of RTD and conventional transistors has attracted much attention for high-speed digital circuit application.

In this paper, we present the design, fabrication and the experimental result of high-speed digital circuit using RTD as load element.

2. Process technology

To fabricate high-speed digital circuit utilizing RTD's NDR characteristic, we integrated AlAs / InGaAs / InAs RTD and InAlAs / InGaAs HEMT monolithically. The epitaxial layers were grown by MBE and the devices were fabricated using optical lithography, e-beam lithography and lift-off process. The cutoff frequency (fT) is about 170 GHz. The threshold voltage (Vth) is -0.6 V, and the maximum transconductance is about 1.05 S/mm. The peak voltage of RTD is 0.17 V, and the peak-current density is $5.5x10^4$ A/cm^2, and the PVCR is about 9. Fig. 2 shows the I-V characteristics of the fabricated RTDs. The current density is normalized for various RTD sizes.

As operation speed increases, the interconnection line effects affect circuit operation. To minimize interconnection line effect, we used high-speed interconnection technology utilizing low-k dielectric BCB (Benzocyclobutene).

Fig. 2. shows the cross-sectional view of the fabricated IC.

3. Circuit design and Measurement

Resonant Tunneling Diodes (RTDs) exhibit negative differential resistance(NDR) characteristics and picosecond level switching time (1.5 ps) [2]. NDR characteristic provides possibility of reducing circuit complexity and power consumption. RTD's very fast switching characteristics provides possibility of high-speed operation.

Utilizing RTD's characteristics we designed and fabricated high-speed static inverter and basic logic gates.

3.1. Static inverter and 3-stage ring oscillator

The schematic of the RTD/HEMT inverter and the load-line diagram is shown in Fig.3. When the input is low (near the threshold voltage of the HEMT), no current can flows through HEMT. Because the current through RTD is also zero, no voltage drop occurs across RTD and the output voltage is VDD (Operation point is around A). When the input is high and the current of HEMT is larger than RTD's peak current, the operation point jumps to B (Second positive resistance region of RTD). The dashed line shows the load-line of conventional inverters.. Comparing operation point B and C, the operation current of RTD-load inverter at high input state is much lower than conventional load-device. So the power consumption of RTD/HEMT inverter is reduced than conventional inverters.

By cascading 3-inverters, RTD/HEMT ring oscillator is designed and fabricated. Fig. 4 shows the measurement result of fabricated 3-stage ring oscillator. The oscillation frequency of the fabricated RTD/HEMT 3-stage ring oscillator is 18.61 GHz. Therefore the delay per gate is less than 8 psec. So we can expect over 60 Gbps operation of digital circuits using RTD/HEMT technology. Because of the nonlinear characteristics of RTD (transition from A to B through NDR region of RTD) the output waveform is not a symmetric sinusoidal wave

3.2. DCFL logic gate using RTD as load element

We designed DCFL logic gate using RTD as load element. Fig. 4. shows the schematic of RTD-based DCFL NOR and NAND gate. The operation principle is similar to conventional FET DCFL circuits. But RTD-based DCFL logic gate can achieve high-speed operation and low power consumption compared to FET-based DCFL logic gate.

Fig. 5. shows the12.5 Gbps patterned input bit stream (11101110) and the output waveform. The output swing is about 200 mV. Because of our measurement system limit, we fed logic low level dc voltage to one input port and fed bit stream to another input port. Fig. 6 shows the eye diagram of NOR gate for 10Gpbs 2^{31}-1 PRBS (pseudo-random bit stream) input data. We can see clear eye opening for the RTD-based NOR gate at 10Gbps.

5. Conclusion

We monolithically integrated InP-based RTDs and HEMTs using conventional process. We designed and fabricated static inverter and 3-stage ring oscillator using RTD as load element. The oscillation frequency is 18.61 GHz. We can expect over 60Gbps operation of digital circuits using RTD as load element from this result.

We also designed and fabricated DCFL logic gate using RTD as load element. The measurement result shows the clear eye opening at 10 Gbps with 200mV swing.

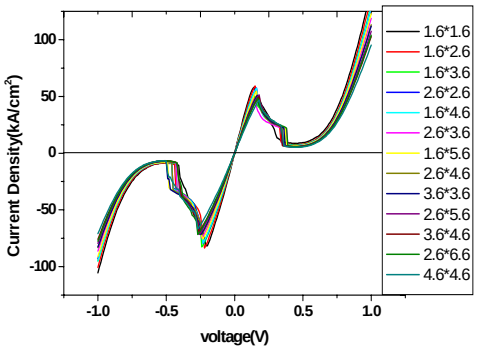

Fig. 1 I-V characteristics of the fabricated RTDs. The peak voltage was 0.17 V , and the current density was $5.5x10^4$ A/cm^2, and the PVCR was about 9.

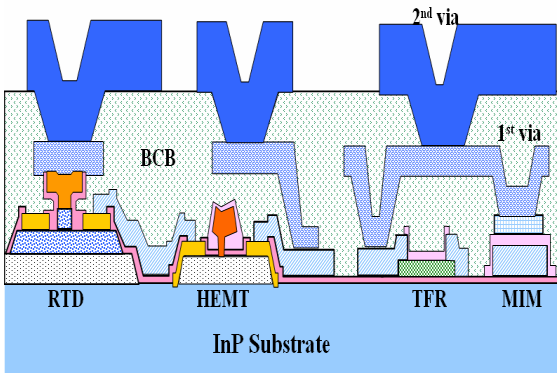

Fig. 2 Cross sectional view of the fabricated IC.

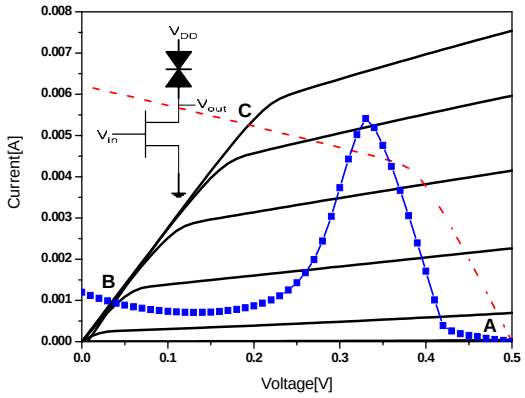

Fig. 3 Schematic diagram of RTD/HEMT and the load lien of RTD/HEMT inverter.

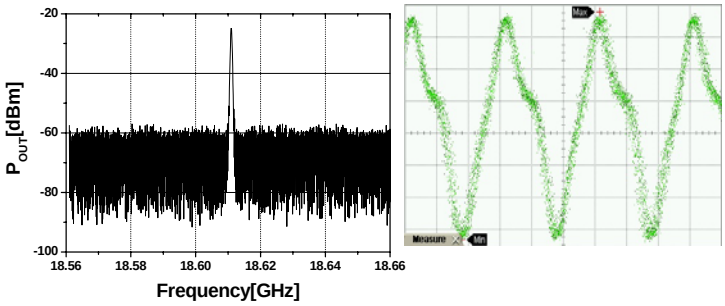

Fig. 4 Measurement result of 3-stage ring oscillator

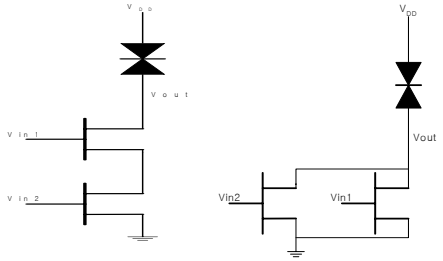

Fig. 5 Schematic diagram of RTD-base logic gate

Fig. 5 Measurement result of NOR gate

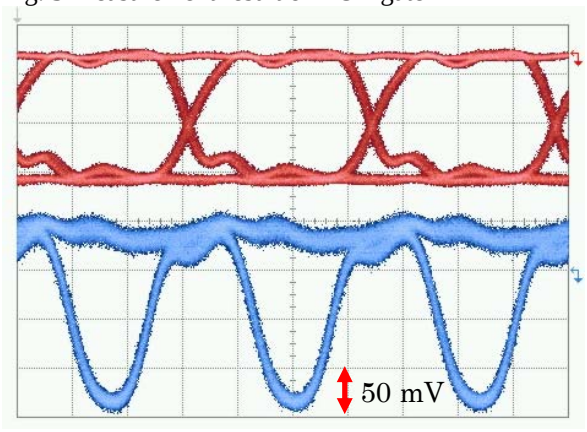

Fig. 6 Eye diagram of NOR gate

Acknowledgements

This work was financially supported by the National program for Tera-HZ Level Integrated Circuits of the Minister of Science and Technology as one of the 21st Century Frontier program

References

[1]K. Maezawa, “A new resonant tunneling logic gate employing monostable-bistable transition.” Jpn. J. Appl. Phys., 1993

[2] N. Shimizu, “In0.53Ga0.47As/AlAs resonant tunneling diodes with switching time of 1.5ps”, Electronic Letters, 1995