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I-2-6

Low leakage gate current of InP transistors with hot electron extracted by attractive potential around i-InP/metal gate

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1. Introduction

When carriers pass through only an intrinsic semiconductor, the propagation delay can be reduced through reduction of scattering in the electron. To realize the carrier transport in intrinsic semiconductor, we proposed and have fabricated a hot electron transistor with a metal gate [1,2] as shown in Fig.1. In this device, forward biased gate affects the potential of the tunneling emitter, results in extraction of the electron passing through only an intrinsic semiconductor. Although forward biased gate has possibility of leakage current, small gate leakage current can be expected by reduced scattering of ballistic electron and little quasi-equilibrium electron in intrinsic semiconductor.

In this report, low leakage current of InP hot electron transistors was exhibited. Common-emitter characteristics showed transistor action of the device controlled by gate bias. Ratio between gate current and collector current had dependence on gate bias.

2. Device fabrication

An i-InP buffer layer (120 nm), n-GaInAs subcollector layer (120 nm), an i-GaInAs spacer layer (10 nm), an i-InP carrier transit (collector) layer (250 nm), a double-barrier structure, an i-GaInAs layer (5.5 nm), and an n-GaInAs emitter layer (90 nm) were grown on a semi-insulating InP substrate by metalorganic vapor phase epitaxy at first. The double-barrier structure consisted of an AlAs barrier layer (4.1 nm), a GaInAs well layer (6.8 nm) and an AlAs barrier layer (4.1 nm). To fabricate emitter mesa, 40 nm wide Cr/Au/Cr (10 nm / 30 nm / 10 nm thick) stripes were fabricated by electron beam lithography and liftoff process. By using the stripe as etching mask, emitter mesa was fabricated by CH_4/H_2 RIE, followed by wet etching to undercut the mesa for isolation between emitter and gate metal. As a result, emitter mesa width became 25 nm. Emitter length was 10 μm. Gate metal was also fabricated to surround the emitter. After formation of collector contact by etching and evaporation, intrinsic device became a mesa structure by wet etching for isolation. Undercut air-bridged wiring for emitter and gate were fabricated simultaneously. Just before the measurement, oxidized surface was removed by diluted hydrochloric acid.

3. Measurements

Current-voltage characteristics were measured at 30 K. By narrowing of emitter mesa and surrounding gate, emitter current (I_E) was controlled by gate-emitter voltage (V_{GE}) and dependence on collector emitter voltage (V_{CE}) became weak. $(\Delta I_E/\Delta V_{GE})$ / $(\Delta I_E/\Delta V_{CE})$ was 6.5 at V_{CE} ~ 2 V and V_{GE} ~ 0.6V. This is reasonable when we take estimated ratio of 8 by calculated effective field from designed structure and strong non-linearity in this bias range into account. $(\Delta I_E/\Delta V_{GE})$ / $(\Delta I_E/\Delta V_{CE})$ was 25 at V_{CE} ~ 2 V and V_{GE} ~ 1.5V.

Gate current (I_G), collector current (I_C) and ratio between I_G and I_C (I_G/I_C) were observed as shown in Fig. 2 and 3 at $V_{GE}=V_{CE}$ to eliminate effect of leakage current between gate and collector. As shown in Fig.3, I_G/I_C had a lowest at V_{GE}=0.8V and lowest I_G/I_C was 0.04. Although V_{GE} for lowest I_G/I_C was changed by each device and surface treatment, observed lowest I_G/I_C was around 1 V. Common-emitter I_C, I_G and I_G/I_C were shown in Figs. 4-6. As shown in Fig. 4, the fabricated device showed conventional transistor action when V_{CE} > 0.6 V. Bias range for I_G < one tenth of I_C was wide as shown in Fig. 6.

As shown in Fig. 5, observed I_G at V_{CE} ~ 0 was larger than saturated I_C in Fig.4. This is due to direct leak current between gate and collector. Present collector barrier is around 0.23 eV because we used band-discontinuity between GaInAs and InP. Moreover, degenerated Fermi level of n-GaInAs subcollector lowers the height. Thus thermionic emission injected from collector becomes large at $V_{GE}>V_{CE}$.

4. Discussions

To reduce leakage current, increase of metal barrier height and increase of collector barrier height are required. On the other hand, observed current level was around several nA and current density was several A/cm^2. Because reported maximum peak current density in resonant tunneling diode with same material system [3] was over 500 kA/cm^2, we can increase current by several order of magnitude when we change emitter barrier thickness and carrier concentration of emitter. As the change of emitter structure does not affect to the leakage current, we can reduce I_G/I_C relatively by increase of I_C. Higher current density is also desirable for high speed operation [1].

The temperature of the device was 30 K. This temperature is for reduction of thermionic emission from the collector barrier. Because scattering of hot electron is not so affected by the temperature until room temperature, relative reduction of I_G will open the operation at room temperature, too.

5. Conclusions

Low leakage current of InP hot electron transistors was exhibited. By using the device with 25 nm wide emitter surrounded by gate metal, common-emitter characteristics showed transistor action of the device controlled by gate bias. I_G/I_C had dependence on gate bias and lowest ratio at $V_{GE}=V_{CE}$ was 0.04 at V_{GE}= 0.8 V.

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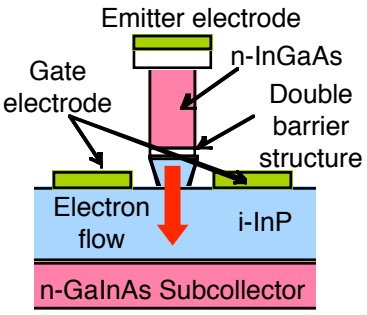

Fig.1 Schematic cross-section of fabricated devices.

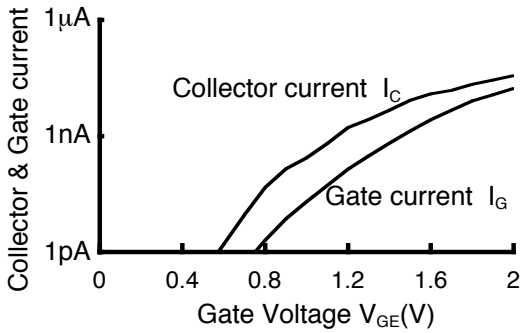

Fig.2 Gate current and collector current at $V_{GE}=V_{CE}$.

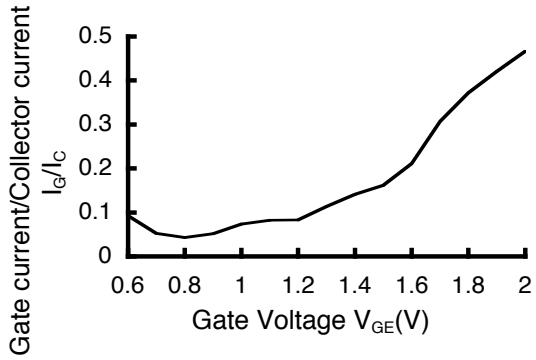

Fig.3 Ratio between gate current and collector current at $V_{GE}=V_{CE}$.

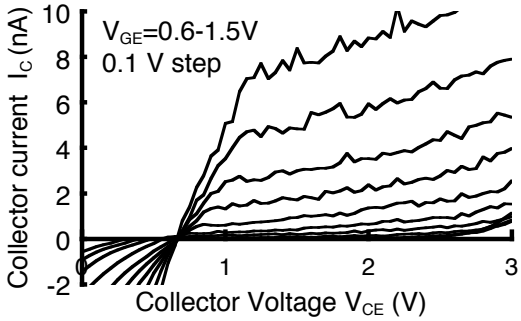

Fig.4 Common emitter I_C-V_{CE} characteristics.

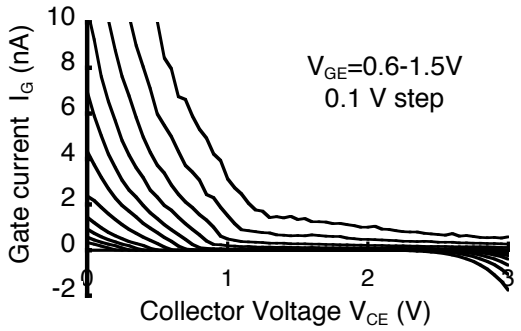

Fig.5 Common emitter I_G-V_{CE} characteristics.

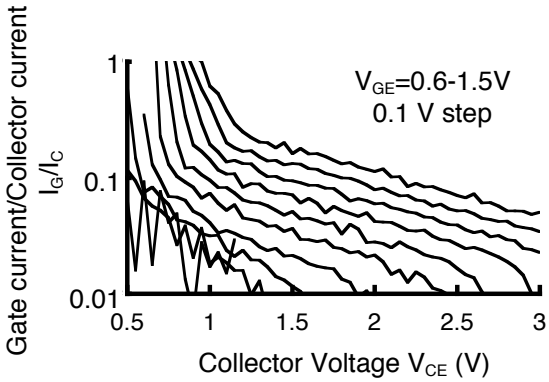

Fig.6 Ratio between gate current and collector current at common emitter configuration.