Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.1060-1061

I-7-4

Theoretical Analysis of Breakdown Characteristics for Recessed Gate GaAs MESFETs

Takashi Shugo, Dumarpa Macarambon Jr., and Masaaki Kuzuhara

Department of Electrical and Electronics Engineering
University of Fukui
3-9-1 Bunkyo, Fukui 910-8507, Japan
Phone: +81-776-27-9714, Fax: +81-776-27-8749, Email: kuzuhara@fuee.fukui-u.ac.jp

1. Introduction

A GaAs-based power FET is widely employed as a transmitter amplifier for a variety of wireless communication systems. It is known that adoption of a recessed gate structure effectively minimizes the source parasitic resistance, resulting in high gain and high efficiency characteristics at high frequencies. However, no studies have been made concerning the effect of gate recessing on the breakdown behavior of GaAs power FETs.

In this work, we theoretically examined the effect of recessed gate structure on the electric field distribution between gate and drain using 2D device simulation. The results indicated an interesting conclusion that the breakdown voltage of the recessed gate FET increased or decreased with increasing the recess depth, depending on the amount of surface negative charge density.

2. Simulation

Figure 1 shows the schematic structure of a GaAs MESFET. We chose the gate length (Lg) and the channel donor concentration (Nd) to be 0.45μm and $2x10^{17}cm^{-3}$, respectively. The threshold voltage calculated was about -4V. The gate voltage was -8V to ensure pinch-off conditions and the drain voltage was fixed at 20V. Negative charges were uniformly distributed on the recess surface with a concentration (Nss) of $0\sim3x10^{12}$ cm^{-2}. The device characteristics were calculated by solving Boltzmann equation using Monte Carlo algorithm coupled with Poisson equation. The model incorporates analytical Γ-L-X band structures with nonparabolicity for GaAs [1].

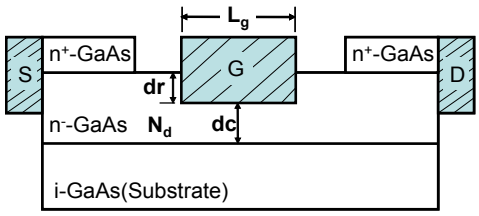

Fig.1 Schematic GaAs MESFET structure.

3. Results

Figure 2 illustrates the maximum electric field as a function of the recess depth. A maximum electric field is observed at the drain side of the gate edge for all Nss values assumed. From Fig.2, the following conclusions were drawn. (1) The maximum electric field is greatly reduced with an increase in Nss. (2) The maximum electric field is alleviated with increasing the recess depth for $Nss<10^{12}$ cm^{-2}. (3) Conversely, the increase in maximum electric field is observed with increasing the recess depth for $Nss>3x10^{12}cm^{-2}$. (4) The maximum electric field converges to 1500kV/cm regardless of the surface negative charge density.

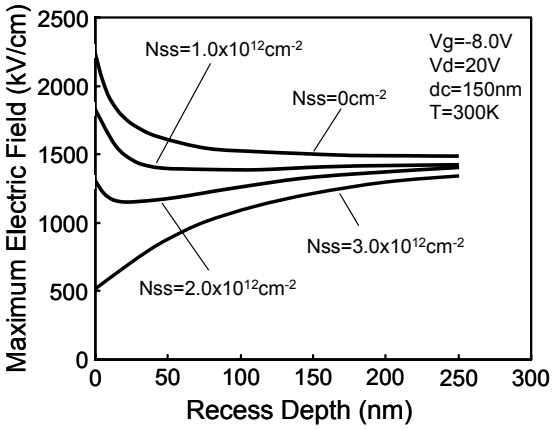

Fig.2 Dependence of maximum electric field on recess depth for various Nss values.

4. Discussion

As already known [2] [3], the electric field is alleviated at the gate edge when the surface negative charge density is increased (see Fig.3). This is because the major part of electric field lines arising from positive donors in the depletion region are terminated at the semiconductor surface having a high density of negative charges.

Figure 4 shows how the maximum electric field is relaxed with increasing the recess depth in the absence of surface negative charges ($Nss<1x10^{12}cm^{-2}$). Since electric field lines are terminated at the side surface as well as at the bottom surface of the gate, the increase in the recess depth leads to relief in the maximum electric field. This is equivalent to an enlargement in the effective gate length which determines the high-field value near the gate. The situation, however, becomes inverted when there is a high density of negative charges on the semiconductor surface. As is shown in Fig.5, significant part of electric lines of force arising from ionized donors are terminated at the surface negative charges, and hence only minor part of electric field lines contributes to the gate field. Under these situations, the maximum electric field increases with increasing the recess depth, as shown in Fig.2.

For a recess depth beyond 200nm, the maximum electric field becomes independent of the surface charge density, resulting in a converged value of 1500kV/cm.

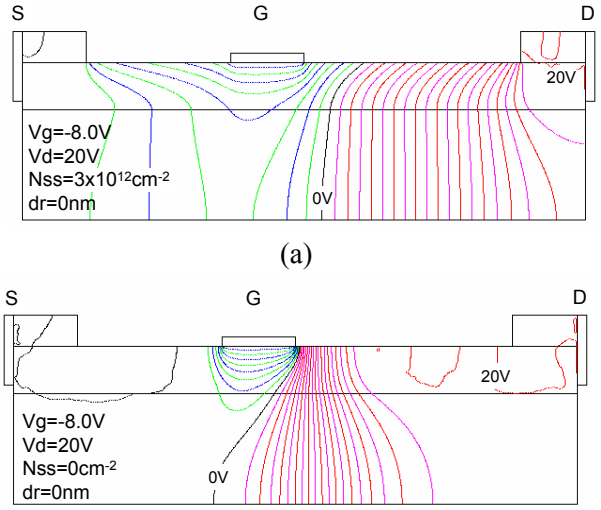

Fig.3 Potential distribution of planar FETs.

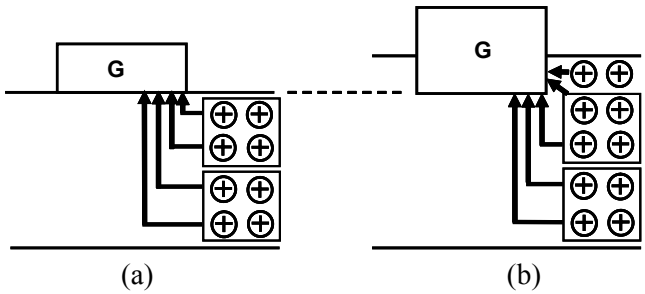

Fig.4 Effect of gate recess on electric lines of force for $Nss=0cm^{-2}$.

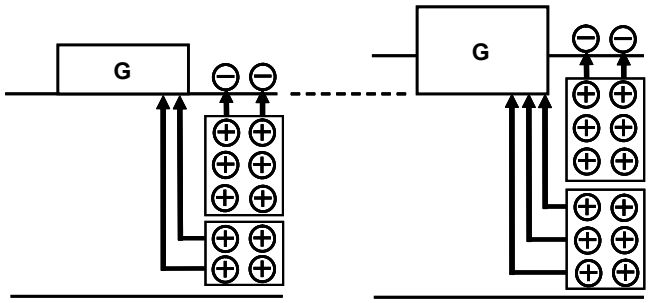

Fig.5 Effect of gate recess on electric lines of force for $Nss=3x10^{12}cm^{-2}$.

5. Conclusion

Breakdown characteristics for a recessed gate GaAs MESFET have been analyzed using 2D device simulation. It was found that introducing a recessed gate structure gives a beneficial or harmful effect on the gate breakdown behavior, depending on the density of surface negative charges.

References

[1] M. Kuzuhara, T. Itoh and K. Hess, Solid-State Electron., 32, 1857 (1989).

[2] S. H. Wemple, W. C. Niehaus H. M. Cox, J.V. Dilorenzo, and W. O. Schlosser, IEEE Trans. Electron Devices, ED-27, 1013 (1980).

[3] H. Mizuta and K. Yamaguchi, IEEE Trans. Electron Devices, ED-34, 2027 (1987).