Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.1062-1063

I-8-1

Analysis of Trap-Parameter Dependence of Lag Phenomena and Current Collapse in GaN FETs

H. Takayanagi, H. Nakano, K. Itagaki and K. Horio

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Minuma-ku, Saitama 337-8570, Japan
Phone: +81-48-687-5813, Fax: +81-48-687-5198, E-mail: horio@sic.shibaura-it.ac.jp

GaN-based FETs are now receiving great interest because of their potential applications to high power and high temperature microwave devices [1]. However, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [2]. This is called drain lag or gate lag, and is problematic in circuit applications. The slow transients mean that the dc *I-V* curves and the ac *I-V* curves become quite different, resulting in lower ac power available than that expected from the dc operation [1],[2]. This is called power slump or current collapse in the GaN-device field. These are serious problems, and there are many experimental works reported on these phenomena. But, only a few theoretical works have been reported for GaN-based FETs [3]-[5], although several numerical analyses were made for GaAs-based FETs [6]-[10]. Therefore, in this work, we have made systematic transient simulations of GaN MESFETs in which deep levels in a semi-insulating buffer layer are considered, and studied how the lag phenomena and pulsed *I-V* curves (current collapse) are affected by the deep-level parameters and the applied drain bias.

Fig.1 shows a device structure analyzed in this study. As a model for the semi-insulating buffer layer, we use a three level compensation model which includes a shallow donor, a deep donor and a deep acceptor. Some experiments show that two levels ($E_C - 1.75$ eV, $E_C - 2.85$ eV) are associated with current collapse in GaN-based FETs with a semi-insulating buffer layer [2], so that we use energy levels of $E_C - 2.85$ eV (or $E_V + 0.6$ eV) for the deep acceptor and of $E_C - 1.75$ eV for the deep donor. Other experiments show shallower energy levels for the deep donor [11],[12], and hence we vary the deep donor's energy level (E_{DD}) as a parameter. Here, the deep-donor density (N_{DD}) and the deep-acceptor density (N_{DA}) are typically set to $5\text{x}10^{16}$ cm^{-3} and $2\text{x}10^{16}$ cm^{-3}, respectively. The shallow donor density in the buffer layer N_{Di} is set to 10^{15} cm^{-3}. The simulator is our in-house program modified from that for GaAs MESFETs [10].

Fig.2 shows calculated drain-current responses when the drain voltage V_D is raised abruptly from 0 V to 20 V or when V_D is lowered from 20 V to 6 V, where the gate voltage V_G is kept constant (0 V). Here, three cases with different $E_C - E_{DD}$ are shown. When V_D is raised, the drain currents overshoot the steady-state values, because electrons are injected into the buffer layer, and the deep traps there need certain time to capture these electrons. On the other hand, when V_D is lowered, the drain currents remain at low values for some periods and begin to increase slowly, showing drain lag behavior. This is due to the slow response of the deep donor. It is understood that the drain currents begin to increase as the deep donors begin to emit electrons, so that the response is faster for shallower E_{DD}. These drain lags are also reported experimentally in GaN MESFETs and HEMTs [2],[3].

We have next calculated a case when V_D and V_G are both changed abruptly from an off point. Fig.3 shows calculated turn-on characteristics when V_G is changed from the threshold voltage V_{th} to 0 V. The off-state drain voltage V_{Doff} is 20 V, and the parameter is the on-state drain voltage V_{Don}. The characteristics are similar to those in Fig.2 where V_D is lowered, and hence the change of V_D (drain lag) is regarded as essential in this case. Fig.4 shows calculated I_D-V_D curves. In this figure, we plot by point (x) the drain current at $t = 10^{-8}$ s after the gate voltage is switched on. This is obtained from Fig.3, and this curve corresponds to a quasi-pulsed *I-V* curve with pulse width of 10^{-8} s. (We are also plotting other quasi-pulsed *I-V* curves when only V_D is changed (cf. Fig.2).) It is seen that the drain currents in the pulsed *I-V* curve are rather lower than those in the steady state. This indicates that current collapse could occur due to the slow response of deep levels in the semi-insulating buffer layer. This type of current reduction is commonly observed experimentally in GaN-based FETs.

Next, we have studied the dependence of deep-level densities (N_{DD}, N_{DA}) in the buffer layer. The above characteristics are found to be almost independent of the deep-donor density N_{DD} under a condition that N_{DD} is higher than N_{DA}. This is because in this condition, the ionized deep-donor density N_{DD}^+, which acts as an electron trap, becomes nearly equal to N_{DA} under equilibrium [6]. Therefore, we will show N_{DA} dependence of the characteristics. Fig.5 shows calculated I_D-V_D curves for different N_{DA}, where N_{DD} is $2\text{x}10^{17}$ cm^{-3}. It is seen that the steady-state drain currents are higher for lower N_{DA}, because the current via the buffer layer becomes higher. It is also clearly seen that the current reduction in the pulsed *I-V* curves is more pronounced for higher N_{DA}. This is because the trapping effects become more significant for higher N_{DA} because of higher N_{DD}^+. It is concluded that the deep-acceptor density in the buffer layer must be made low to minimize the current reduction or current collapse.

Finally, we have studied dependence of off-state drain voltage V_{Doff} on the current collapse. Fig.6 shows calculated pulsed *I-V* curves as a parameter of V_{Doff}. It is seen that the current reduction (current collapse) is more pronounced for higher V_{Doff}. This is understood from the fact that in the case of higher drain bias, electrons are injected deeper into the buffer layer and more electrons are captured by the traps. Therefore, when the drain voltage is lowered from higher V_{Doff}, the trapping effects are more pronounced, resulting in the heavier current reduction. This tendency is also reported experimentally in AlGaN/GaN HFETs [13].

In summary, two-dimensional transient analyses of GaN MESFETs have been performed in which a three level compensation model is adopted for the semi-insulating buffer layer, and the pulsed *I-V* curves have been derived from the transient characteristics. It has been shown that the current collapse (current reduction) becomes more pronounced when the deep-acceptor density in the buffer layer is higher and when the off-state drain voltage is higher, because the trapping effects become more significant. The buffer-trapping effects may be similar to trapping effects in an undoped GaN layer in AlGaN/GaN HEMTs. It is suggested that to minimize the current collapse in GaN-based FETs, the acceptor density in a semi-insulating GaN layer should be made low.

[1] U. K. Mishra, P. P. Parikh and Y.-F. Wu, Proc. IEEE **90** (2002) 1022.
[2] S. C. Binari, P. B. Klein and T. E. Kazior, Proc. IEEE **90** (2002) 1048.
[3] G. Meneghesso et al., IEEE Trans. Electron Devices **51** (2004) 1554.
[4] N. Braga et al., *Proceedings of Compound Semiconductor IC Symposium* (2004) 287.
[5] K. Horio and K. Yonemoto, *Proceedings of 12th European Gallium Arsenide & Other Compound Semiconductors Application Symposium* (2004) 567.
[6] K. Horio and Y. Fuseya, IEEE Trans. Electron Devices **41** (1994) 1340.
[7] S. H. Lo and C. P. Lee, IEEE Trans. Electron Devices **41** (1994) 1504.
[8] K. Kunihiro and Y. Ohno, IEEE Trans. Electron Devices **43** (1996) 1336.
[9] G. Verzellesi et al., IEEE Trans. Electron Devices **50** (2003) 1773.
[10] Y. Kazami, D. Kasai and K. Horio, IEEE Trans. Electron Devices **51** (2004) 1760.
[11] W. Kruppa, S. C. Binari and K. Doverspike, Electron. Lett. **31** (1995) 1951.
[12] H. Morkoc, *Nitride Semiconductors and Devices*, Springer-Verlag (1999).
[13] A. Koudymov et al., IEEE Electron Device Lett. **24** (2003) 680.

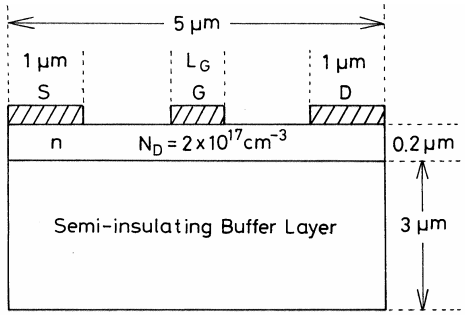

Fig.1 Modeled GaN MESFET analyzed here.

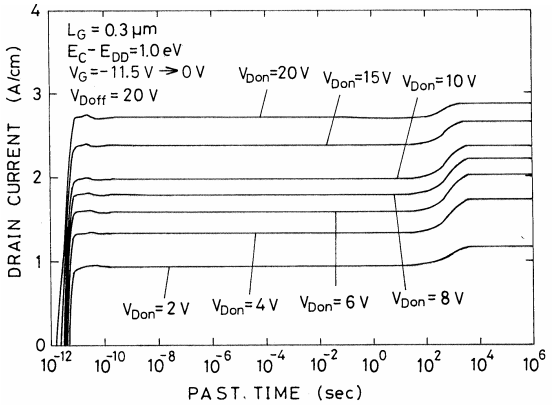

Fig.3 Calculated turn-on characteristics of GaN MESFET when V_G is changed from threshold voltage V_{th} to 0 V, with on-state drain voltage V_{Don} as a parameter. V_{Doff} = 20 V. $E_C - E_{DD}$ = 1.0 eV. $N_{DD} = 5 \times 10^{16}$ cm^{-3} and $N_{DA} = 2 \times 10^{16}$ cm^{-3}.

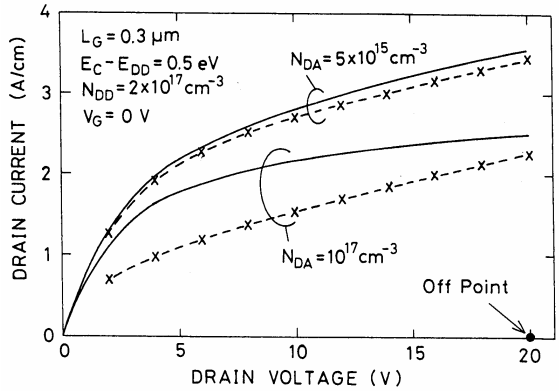

Fig.5 Steady-state *I-V* curves (V_G = 0 V; solid lines) and quasi-pulsed *I-V* curves (x ; $t = 10^{-8}$ s) for GaN MESFETs with different N_{DA} (5×10^{15} cm^{-3} , 10^{17} cm^{-3}). Initial point is shown by (●). $E_C - E_{DD}$ = 0.5 eV and $N_{DD} = 2 \times 10^{17}$ cm^{-3}.

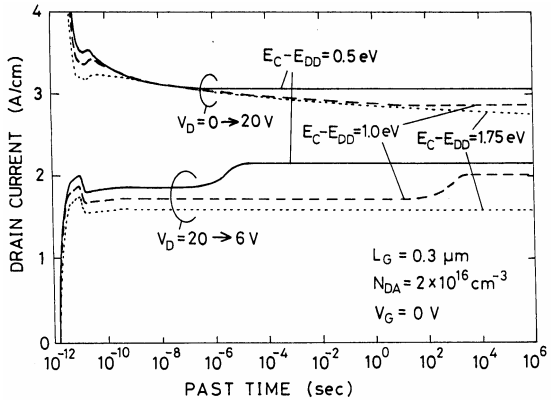

Fig.2 Comparison of drain-current responses of GaN MESFET as a parameter of deep donor's energy level E_{DD} when V_D is raised abruptly from 0 V to 20 V (upper) or when V_D is lowered abruptly from 20 V to 6 V (lower). $N_{DD} = 5 \times 10^{16}$ cm^{-3}.

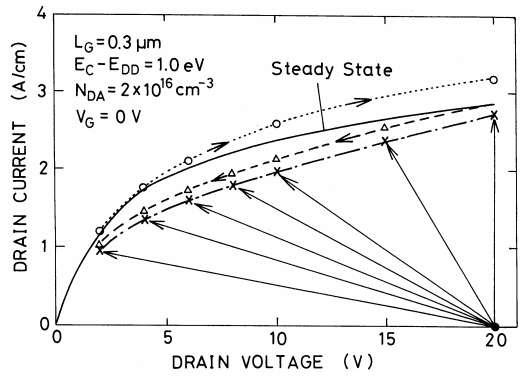

Fig.4 Steady-state *I-V* curve (V_G = 0 V; solid line) and quasi-pulsed *I-V* curves for GaN MESFET. $E_C - E_{DD}$ = 1.0 eV. (x): V_{Doff} = 20 V and $V_{Goff} = V_{th}$ ($t = 10^{-8}$ s; Fig.3), (○): V_D is raised from 0 V ($t = 10^{-9}$ s; Fig.2), (Δ): V_D is lowered from 20V ($t = 10^{-8}$ s; Fig.2).

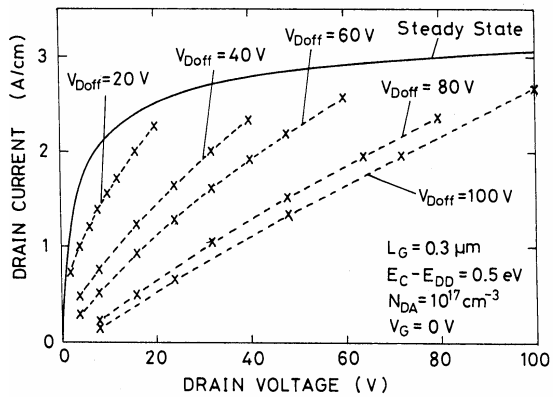

Fig.6 Steady-state *I-V* curve (V_G = 0 V; solid line) and quasi-pulsed *I-V* curves (x ; $t = 10^{-8}$ s) for GaN MESFET, with off-state drain voltage V_{Doff} as a parameter. $E_C - E_{DD}$ = 0.5 eV. $N_{DD} = 2 \times 10^{17}$ cm^{-3} and $N_{DA} = 10^{17}$ cm^{-3}.