Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.1066-1067

I-8-3

Noise Analysis of Nitride-based MOS-HFETs with Photo-chemical Vapor Deposition SiO_2 Gate Oxide in the Linear and Saturation Region

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1. Introduction

Recently, we reported the fabrication of high performance nitride-based MOS-HFETs with photo-CVD SiO_2 as the insulator material [1]. Low frequency noise is one of the most important parameters of microwave devices. Previously, Rumyantsev et al. reported a study on low frequency noise of nitride-based FETs when the FETs were biased in the linear region [2-4]. However, we need to bias the FETs in the saturation region for practical device applications. A detailed study on the low frequency noise of the fabricated devices biased in the linear and saturation regions will be reported.

2. Experiments

Samples used in this study were all grown by MOCVD on sapphire substrates. The structure of the samples consists of a 30 nm GaN nucleation layer, a 2 μm-thick undoped GaN buffer layer, a 5 nm-thick undoped $Al_{0.22}Ga_{0.78}N$ spacer layer, a 15 nm-thick Si-doped $Al_{0.22}Ga_{0.78}N$ carrier supplying layer ($n=5\times10^{18}$ cm^{-3}) and a 4 nm-thick undoped $Al_{0.22}Ga_{0.78}N$ cap layer. Low frequency noise of the fabricated MOS-HFETs was then measured by biasing these devices in the linear (i.e. V_{ds}=3V) and saturation region (i.e. V_{ds}=12V), respectively, with various gate bias voltages in the frequency range from 1 to 10 kHz.

3. Results and Discussion

A. Linear Region:

Figure 1 shows noise of the devices depends strongly on the gate voltage. On the other hand, these spectra could be fitted well by 1/f law. Figure 2 shows noise increased slightly as the temperature increased. Such a result suggests noise in our MOS-HFETs was dominated by 1/f noise while generation-recombination noise in the devices was negligibly small. Figure 3(a) shows room temperature noise of our MOS-HFETs was proportional to V_{gs}^{-1} when $-4V < V_{gs} < 0V$. On the other hand, noise of these devices was independent of V_{gs} when $0V < V_{gs} < 4V$, as shown in fig. 3(b). Gate leakage current induced noise can be negligibly small. If the contact noise (S_{Rc}) is also small, noise should be dominated only by bulk noise. In other words, noise could be expressed as:

$$\frac{S_I}{I^2} = \frac{S_{Rc} + S_{AlGaN/GaN}}{R_{AlGaN/GaN}^{\ 2}} \cong \frac{S_{AlGaN/GaN}}{R_{AlGaN/GaN}^{\ 2}} \propto \frac{1}{L} \quad \text{----------(1)}$$

where L is the drain-source distance. Figure 4 shows normalized noise power density was indeed inversely proportional to the drain-source distance. Such a relationship indicates that the low frequency noise is dominated only by bulk noise for the fabricated MOS-HFETs.

The total low frequency noise of our MOS-HFETs between source and drain could be given by:

$$S_{R_{total}} = S_{R_{ch}} + S_{R_s} \text{ ----------(2)}$$

On the other hand, the total resistance between source and drain could be given by [5]:

$$R_{total} = R_{ch} + R_s = \frac{L_{gate}\left|V_{off}\right|}{Wq\,\mu n_{ch}(V_{gs} - V_{off})} + R_s \text{ ----------(3)}$$

where R_{ch} is the channel resistance underneath the gate, R_s is the series resistance, L_{gate} is the length of the gate, W is the width of the channel, q is the charge of an electron, μ is the 2DEG mobility, n_{ch} is the 2DEG concentration, and V_{off} is the pinch-off voltage. At $V_{gs} < 0V$,

$$R_{ch} > R_s \quad and \quad S_{R_{ch}} > S_{R_s} \text{ ----------(4)}$$

Thus, S_{Rtotal} were dominated by the contributions from the channel underneath the gate. Therefore,

$$\frac{S_I}{I^2} = \frac{S_{R_t}}{R_t^{\ 2}} = \frac{S_{R_{ch}} + S_{R_s}}{(R_{ch} + R_s)^2} \cong \frac{S_{R_{ch}}}{R_{ch}^{\ 2}}, \quad \frac{S_I}{I^2} = \frac{\alpha_{ch}}{N_{ch} f} \propto V_{gs}^{\ -1} \text{ ------- (5)}$$

On the other hand, at $V_{gs} > 0V$:

$$R_s > R_{ch} \quad and \quad S_{R_s} > S_{R_{ch}} \text{ ----------(6)}$$

Thus, S_{Rtotal} were dominated by the contributions from the parasitic series resistance. Therefore,

$$\frac{S_I}{I^2} = \frac{S_{R_t}}{R_t^{\ 2}} = \frac{S_{R_{ch}} + S_{R_s}}{(R_{ch} + R_s)^2} \cong \frac{S_{R_s}}{R_s^{\ 2}} = \frac{\alpha_s}{N_s f} \propto V_{gs}^{\ 0} \text{ ----------(7)}$$

It can be seen clearly that these theoretical predications agree very well with the experimental results as shown in fig. 3(a) and (b).

It should be noted that the Hooge's coefficient α of the fabricated MOS-HFETs were estimated to be ~10^{-3}. Such values are similar to those reported by S. L. Rumyantsev et al [2-4].

B. Saturation Region:

Figure 5 shows noise power density increased slightly with temperature in the saturation region. Such a result suggested again that g-r noise is negligibly small. Figure 6 shows noise of the devices was also dominated by the 1/f

noise, the 1/f law was valid only up to 100 Hz. Above 100 Hz, noise decreased as $1/f^{\Gamma}$, where $1.1 < \Gamma < 2.3$ for these devices. This could be attributed to the spatial distribution of interfacial trap states. We believe that the interfacial trap states with a long time constant (i.e. below 100 Hz) are uniformly distributed. Thus, 1/f law could be applied when the frequency was lower than 100Hz. In contrast, interfacial trap states with a short time constant (above 100 Hz) are non-uniformly distributed. As a result, we observed a significant deviation from the 1/f law at high frequency [6-7]. Furthermore, it was found that the value of Γ increased from 1.1 at V_{gs}=-8V to 2.3 at V_{gs}=4V for the AlGaN/GaN MOS-HFETs with Photo-CVD SiO_2 gate oxide. Such an increase could be attributed to the trap states inside the oxide layer. Since the spatial trap distribution in these oxide trap states depends strongly on the applied gate bias [8-9], the spatial distribution of the total trap states will change from uniform to non-uniform as we change the applied gate bias.

Figure 7 shows noise power density decreased monotonically with the increase of gate voltage. Such results are different from those observed when the devices were biased in linear region shown in figures 3(a) and 3(b). We tentatively attributed this to the additional noises induced by edge tunneling near the drain side at high drain biases. To clarify this point, a more detailed study on the noise performance of these devices is needed.

4. Summary

Low frequency noise of AlGaN/GaN MOS-HFETs with photo-CVD SiO_2 gate oxide was investigated as functions of gate bias (from V_{gs}=-8V to V_{gs}=4V) both in linear (V_{ds}=3V) and in saturation (V_{ds}=12V) regions. In linear region, it was found that measured noise spectra were fitted well by the 1/f law up to 10 kHz. The normalized noise power density of our MOS-HFETs was proportional to V_{gs}^{-1} when $-4V < V_{gs} < 0V$, and was independent of the gate voltage when $0V < V_{gs} < 4V$. The Hooge's coefficients α_{ch} and α_s of our fabricated MOS-HFETs were estimated to be around 10^{-3}. In saturation region, it was found that measured noise power density decreased monotonically with the increase of gate voltage.

Acknowledgements:

This work was supported by National Science Council under contract number NSC-93-2215-E-006-010 and NSC-93-2215-E-218-013.

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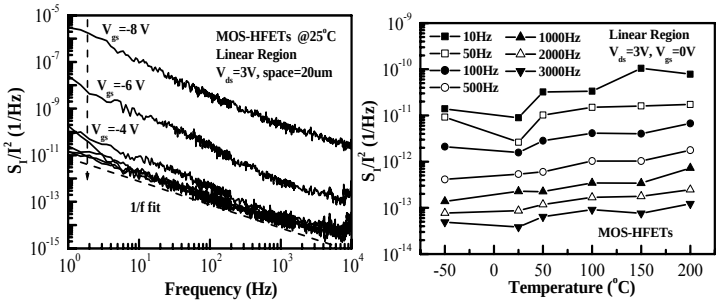

Fig. 1 Room temperature noise spectra in the linear region.
Fig. 2 Temperature dependence of noise at different frequencies in the linear region.

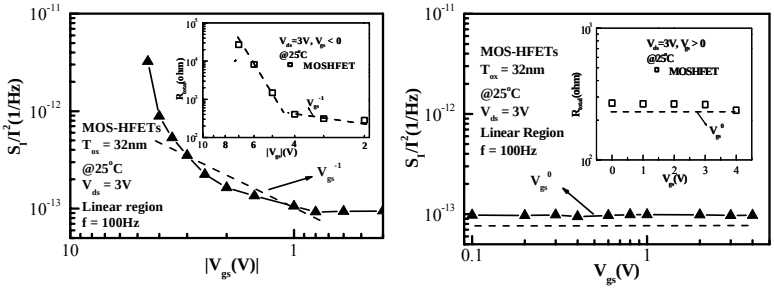

Fig. 3 Room temperature noise as functions of V_{gs} in the linear region at different frequencies, (a)$V_{gs} < 0V$, (b) $V_{gs} > 0V$.

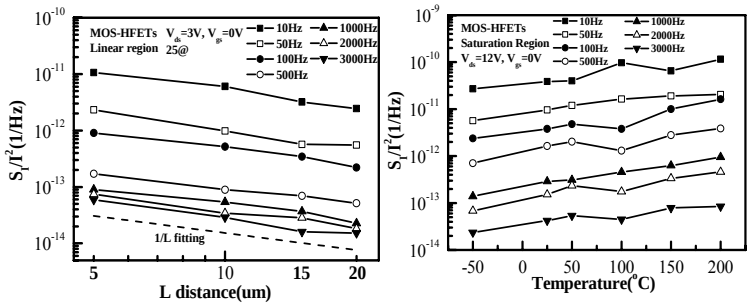

Fig. 4 noise spectra as functions of drain-source distance. These spectra were all measured by biasing in linear region
Fig. 5 Temperature dependence of noise different frequencies in the saturation region.

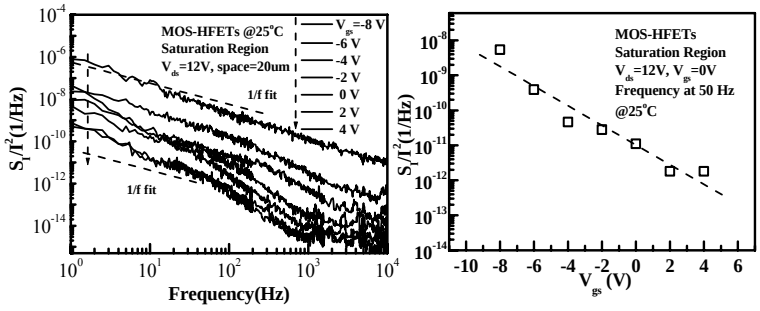

Fig. 6 Room temperature noise spectra in the saturation region.
Fig. 7 noise as functions of V_{gs} in the saturation region.