Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.506-507

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Analysis of NiSi Fully-silicided Gate on SiO_2 and HfO_2 for CMOS Application

Chih Feng Huang[1] and Bing Yue Tsui[1,2]

[1]Department of electronics Engineering, National Chiao-Tung University1001 Ta-Hsueh Road, Hsinchu, Taiwan
Email:bytsui@mail.nctu.edu.tw, Tel: 886-3-5131570, Fax:886-3-5724361
[2]National Nano Device Laboratories, 1001-1 Ta-Hsueh Road, Hsinchu 300, Taiwan, R.O.C

1. Abstract

Work function modulation and thermal/electrical stability of NiSi fully-silicided (FUSI) gate on SiO_2 and HfO_2 are investigated in this work. Fermi-pinning effect on HfO_2 can be relaxed by a SiO_2-like interfacial layer but the effective oxide thickness will increase. The NiSi FUSI gate is stable up to 600°C. Prolonged 600°C annealing degrades gate dielectric due to stress and impurity diffusion.

Keywords : FUSI gate, silicide, Fermi-pinning

2. Introduction

Fully-silicided metal gate has attracted more and more attentions since it was reported in 2001 due to its easy integration with conventional CMOS process and its tunable work function (Φ_m) [1-4]. Wide range Φ_m modulation of doped NiSi gate was also reported so that NiSi FUSI gate is suitable for the single gate CMOSFETs [5]. However, most of the previous works demonstrated the tunable Φ_m on SiO_2 layer only. Although some literatures reported that the Φ_m of pure NiSi gate on Hf-based oxide is free of Fermi-level pinning (FP) problem, the doped NiSi gate is not clearly investigated yet [6]. In this work, we report the FP effect of the doped FUSI gate on HfO_2 and on SiO_2.

3. Experiments

MOS capacitors were fabricated as test devices. Two sets of capacitors were fabricated. One has single SiO_2 layer with thickness of 5.5nm, 10.5nm and 17nm. The other one has HfO_2/SiO_2 stack with thickness combination of 2nm/5.5nm, 2nm/10.5nm, and 2nm/17nm. Some samples, before silicidation, were pre-doped by BF_2^+ implantation and were activated at 900°C for 30sec. The other samples were doped by implant-to-silicide (ITS) method and were annealed at 600°C for 30sec. The process conditions of MOS capacitors are listed in Table I. The flat-band voltage (V_{FB}) and the capacitively equivalent oxide thickness (CET) were determined from the C-V curve measured at 100 KHz. The effective work function ($\Phi_{m,eff}$) was then extrapolated from the V_{FB}-CET plots.

4. Results and discussions

The extracted $\Phi_{m,eff}$ are shown in Fig.1. The NiSi FUSI gate on SiO_2 layer can be modulated from 4.36 eV to 5.14 eV by ITS doping method. This modulation range is similar to that obtained by pre-doping method [1-4]. However, the $\Phi_{m,eff}$ modulation range of the HfO_2 sample is only 0.18 eV by ITS doping method. If the poly-Si is pre-doped by boron, the $\Phi_{m,eff}$ modulation on HfO_2 is still lower than that on SiO_2. Fig.2 shows the SIMS depth profiles of the ITS doped samples. It is clear that both boron and phosphorus pile up at the NiSi/dielectric interface no matter what the dielectric is SiO_2 or HfO_2. Although the boron ion intensity at the NiSi/HfO_2 is slightly lower than that at the NiSi/SiO_2 interface, the intensities of phosphorus ions at both interfaces are identical. Therefore, the FP effect on HfO_2 layer can not be explained by the extent of dopant pileup.

Fig.3 shows the interface structure of the NiSi/HfO_2 sample inspected by transimission electron microscopy (TEM). A thin interfacial layer (IL) is observed on both samples. The IL is thick and continuous for the pre-doped sample while it is discontinuous for the ITS doped sample. To identify the atomic composition of the IL, NiSi is selectively removed by HF+IPA solution to expose the IL. Fig.4 compares the XPS spectra on the IL surface (after NiSi removal) and on the HfO_2 surface (after IL removal). Because the IL is very thin, Hf-O signals are detected at both surfaces. The O_{1S} binding energy shifts from Si-O binding energy to Hf-O binding energy as the analyzed surface changes from IL to HfO_2. Moreover, no Hf-Si signal is detected. These results indicate that the IL is a SiO_2-like material but not Hf-silicate-like material. The IL layer might be formed during a-Si deposition and post-annealing. The uniform SiO_2-like IL of the pre-doped HfO_2 sample can suppress the FP effect but will increase the CET.

Fig.5 shows the XRD spectra of Ni-silicides after annealing at various conditions. The NiSi phase is very stable at 600°C. The sheet resistance of NiSi is about 6 Ω/□ and the CET does not changes at 600°C as shown in Fig.6. The C-V shift under bias-temperature stress at 200°C and ±2MV/cm is negligible as shown in Fig.7. These results imply that the Ni in NiSi is stable under electric field.

Fig.8 shows that the interface state density (D_{it}) of FUSI gate is lower than $1x10^{11}$ $cm^{-2}eV^{-1}$ if the silicide is formed at 500°C. Silicidation at 600°C increases D_{it} to $4x10^{11}$ $cm^{-2}eV^{-1}$. The room temperature thin film stress after silicidation at 500 and 600°C is 7.5 GPa and 9.6 GPa, respectively. It is thus suspected that the D_{it} degradation is due to thermal stress. Fig.9 shows that the prolonged annealing at 600°C increases the magnitude of negative V_{FB} shift and of the hysteresis of C-V curve. After long period 500°C annealing, the C-V curves do not change. It is thus postulated that the degradation comes from both thermal stress and impurity diffusion into gate dielectric.

5. Conclusions

Work function of NiSi FUSI gate on SiO_2 can be modulated by either pre-doping or ITS doping method. Fermi-pinning occurs on HfO_2 sample. It can be relaxed by a SiO_2-like IL but the CET will increase. The NiSi FUSI gate is stable up to 600°C. Prolonged 600°C annealing may degrade gate dielectric due to stress and impurity diffusion.

Acknowledgement

This work was supported by the National Science Council of R.O.C. and ITRI.

References

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Table I Process conditions of MOS capacitors.

		SiO_2 sample	HfO_2 sample
Gate dielectric	Structure	SiO_2	HfO_2 / SiO_2
	Thickness	5.5nm, 10.5nm, 17nm	2nm/5.5nm, 2nm/10.5nm, 2nm/17nm
NiSi doping method		ITS	ITS, Pre-doped
Implantation conditions		BF_2/1E15/10KeV P/1E15/10KeV	BF_2/1E15/10KeV P/1E15/10KeV

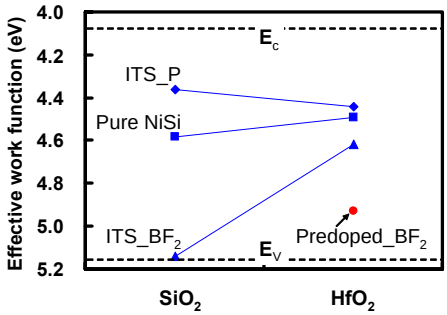

Fig.1 The extracted effective work function ($\Phi_{m,eff}$) of the NiSi FUSI gate on SiO_2 and HfO_2.

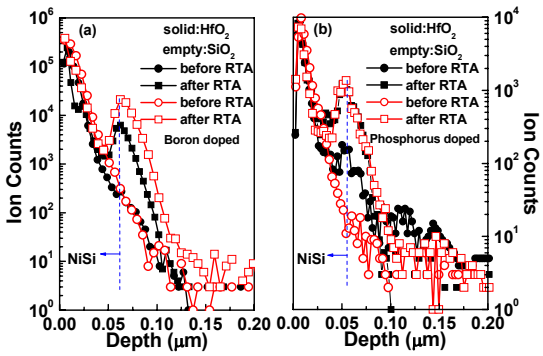

Fig.2 SIMS depth profiles of the ITS doped samples. (a) Boron doped sample and (b) Phosphorus doped sample.

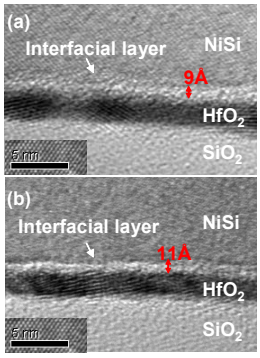

Fig.3 Cross-section of the (a) ITS doped NiSi/HfO_2 sample and (b) pre-doped NiSi/HfO_2 sample.

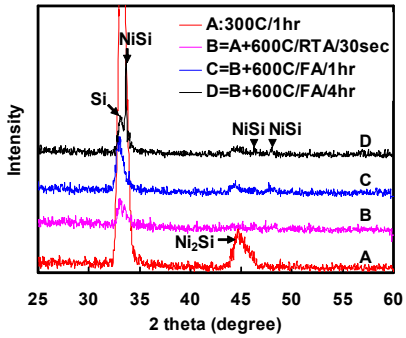

Fig.5 XRD spectra of Ni-silicide after annealing at various conditions.

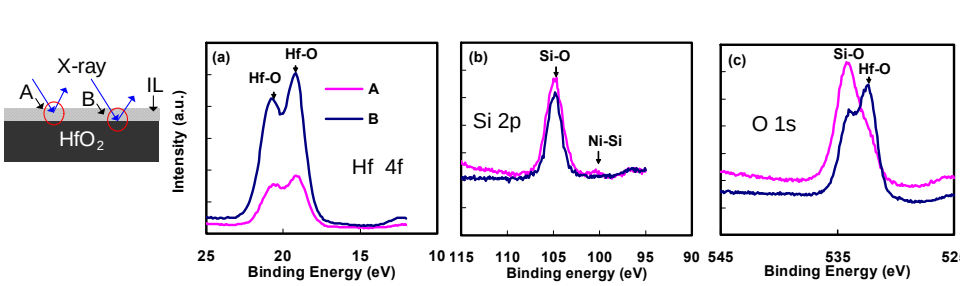

Fig.4 XPS spectra on the IL surface (after NiSi removal) and on the HfO_2 surface (after IL removal).

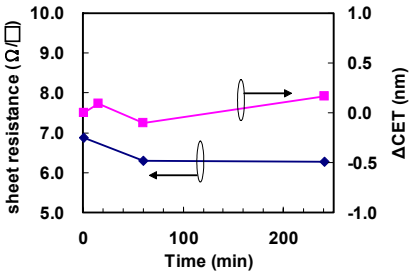

Fig.6 Sheet resistance of NiSi and change of CET as a function of annealing time at 600°C.

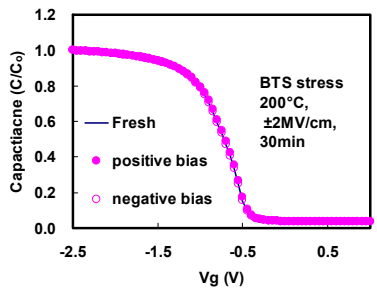

Fig.7 C-V characteristics of a FUSI gate capacitor after bias-temperature stress at 200°C and ±2MV/cm.

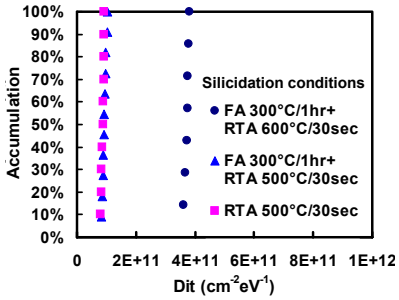

Fig.8 Cumulative distribution of interface state density of FUSI gate capacitors as silicide formed at various conditions.

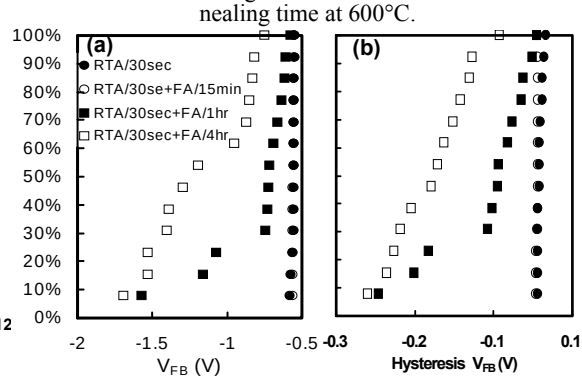

Fig.9 Cumulative distribution of V_{FB} and hysteresis of FUSI gate capacitors as a function of annealing time at 600°C.