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Overcoming Challenges in Metal Gate Etching for Sub-45 nm Technology Node

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1. Introduction

Metal gate electrodes are being investigated as an alternative to polysilicon gate for advanced CMOS in the sub-45 nm regime. Among several candidates, TaN and its alloys have shown potential for use due to their work function tunability and high thermal stability. However, scaling down the gate dimensions to sub-45 nm poses great challenges both for lithography and metal gate etching. The resolution capability of 193 and 248 nm DUV is not sufficient to allow direct patterning of sub-45 nm structures even with introduction of advanced phase-shift masks. Therefore, photoresist (PR) trimming process is required to reduce the feature size. We found that the usage of a dielectric hard mask (HM) is preferable for TaN gate etching due to substantial critical dimensions (CD) gain if etching is carried out with a PR mask. Etching of HM, however, presents a challenge, as a trade-off exists between contradicting requirements of maintaining sufficient selectivity to PR and avoiding formation of excessive sidewall polymer resulting in CD gain. Finally, etching of TaN gate is very challenging due to low volatility of Ta halogenids. Thus, the subject of present work is to develop plasma etching process and integration scheme for patterning of 45 nm TaN gate structure.

2. Experimental

In this study, gate stack was: 90 nm SiN +20 nm SiO_2 + 80 nm TaN on top of 3.5 nm HfAlO gate dielectric. The latter was deposited by atomic layer chemical vapour deposition (ALCVD). Lithography was performed in Nikon 248 nm DUV step and scan system with phase shift mask using a 300 nm-thick DUV resist with organic antireflective coating. Post development CD were 80-85 nm. Integrated process of PR trimming and HM etching was performed in Tokyo Electron Ltd. dipole ring magnetron etcher, followed by PR stripping in Mattson inductively coupled plasma. TaN etching was performed in DPS (decoupled plasma source) metal etch chamber from Applied Materials. All etching steps were optimized by design of experiment (DOE).

3. Results and discussions

Thin initial PR thickness aggravated by 10% post litho thickness loss for critical lines made it necessary to minimize strip to trim ratio in the trim process to provide margin for subsequent HM etch. By DOE it was established that strip to trim ratio decreased with increase of pressure and O_2 concentration in the gas mixture of O_2+N_2 (Fig.1), which is attributed to increase of isotropic component of plasma. After PR trimming, by optimized recipe, to final CD 40-45 nm, still there was sufficient PR thickness for subsequent etching of dual HM (SiN+SiO_2), however, process window should be restricted to a very low power density to avoid thermal stress in PR lines resulting in their bending and eventual collapse. Both SiN and SiO_2 etching steps were optimized and two-step process was engineered: SiN layer was etched up to SiO_2 by end-point in $CHF_3/O_2/Ar$ plasma with relatively high O_2 content to avoid CD gain, while removal of SiO_2 layer was carried out in a mixture of $CHF_3/CF_4/Ar$. It was found that O_2 should be excluded while etching SiO_2 down to TaN surface, as Ta is easily oxidized and low-volatile by-products re-deposited on sidewall resulting in the increased CD gain (Fig.2). Thus, dual HM structure provided advantage of better CD control by timely change of gas mixture composition. The process window, which we established for HM etching, secured profile close to vertical and CD gain not exceeding 5 nm (Fig.3).

Etching of TaN gate on top of 3.5 nm high-k dielectric HfAlO was performed in gas mixture of Cl_2/HBr/Ar [1]. It was found that unlike etching with PR mask, TaN etching with SiN mask may have substantial isotropic component. Increase of HBr content and bias power reduced isotropic etching and allowed to bring undercut value to zero (Fig.4). However, process window is narrow due to onset of sidewall by-product deposition, giving rise to CD gain.

Process conditions for overetch step were separately optimized for maximal selectivity by DOE with three variable factors: HBr/Cl_2 ratio, source and bias power. The selectivity of TaN to HfAlO improves with reducing bias power and HBr content and with increasing source power (Fig.5). As etching with low HBr content has isotropic component, overetch step parameters has been carefully balanced to provide sufficient selectivity and avoid degradation of vertical profile obtained in main etch. Thus, two-step process was developed. Final gate profile with CD less than 45 nm is illustrated by Fig 6. Performance of typical n-MOSFET fabricated using the described process scheme is shown in Figs. 7 and 8.

4. Conclusions

An integration scheme using dual dielectric HM was developed for TaN metal gate etching. Capability of 248 nm DUV lithography was extended to pattern sub 45 nm CD making use of phase-shift mask and PR trimming process. The metal gate etching and integration scheme were validated by successful fabrication and characterization of MOS transistors which confirmed the process feasibility of use of TaN metal gate with HfAlO high-k dielectric for the sub-45 nm technology node.

References

[1] S.I.Yi, S.Nam, K. Huang, P.C.Nallan, US Patent 6638874, B2, publ.28 Oct.2003

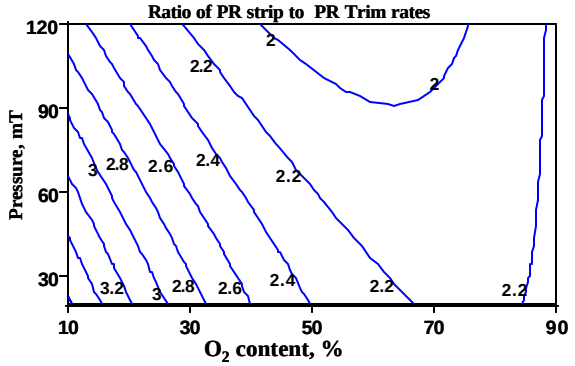

Fig. 1 Minimization of PR strip/PR trim rate ratio by DOE. Optimal parameters: pressure 100-120mT, O_2 content 50-70%

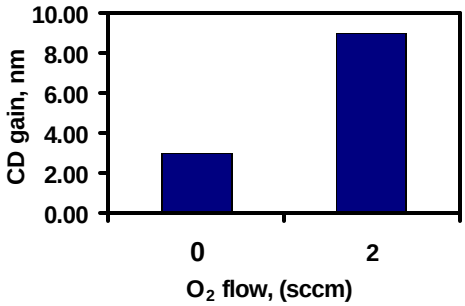

Fig. 2 Effect of added O_2 on CD gain during SiO_2 removal on underlying TaN

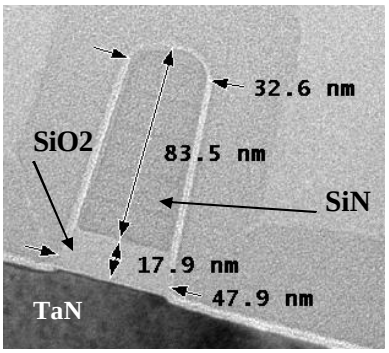

Fig. 3 Sub-50 nm SiN-SiO_2 HM etch profile

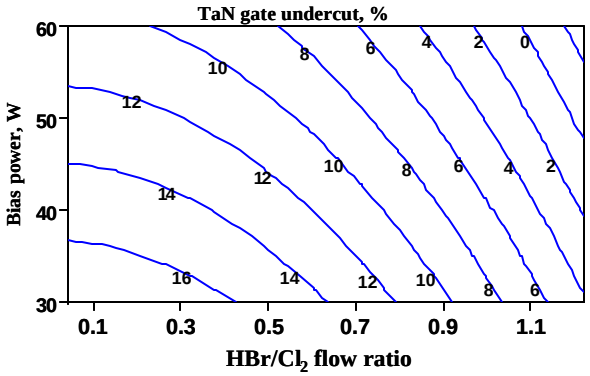

Fig. 4 Undercut of TaN gate versus bias power and HBr/Cl_2 flow ratio

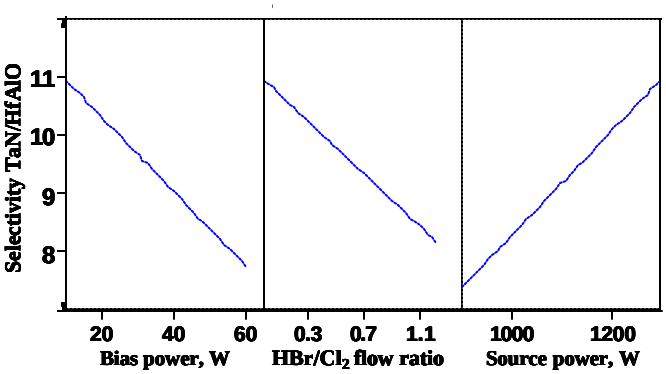

Fig. 5 Selectivity TaN/HfAlO versus process parameters

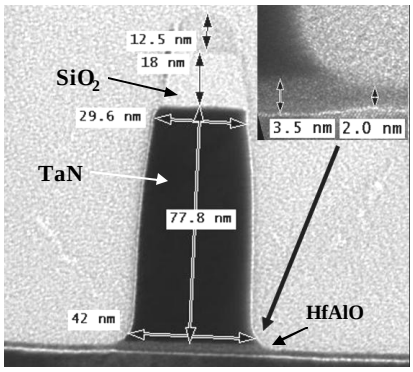

Fig. 6 Sub-45 nm TaN gate on HfAlO dielectric post etch

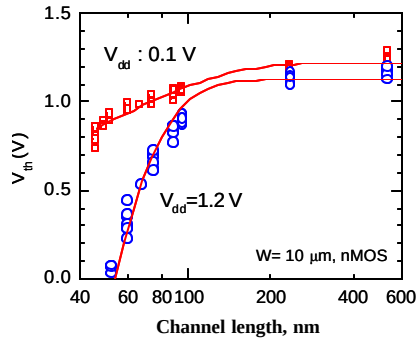

Fig. 7 Threshold voltage versus gate channel length

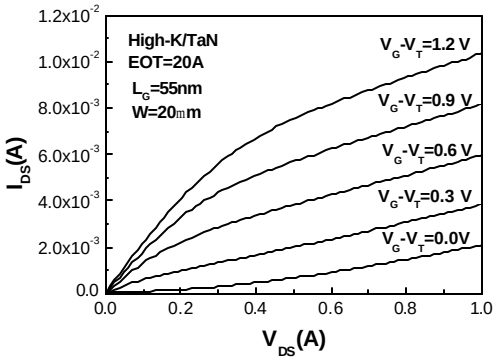

Fig. 8. Drain current-voltage characteristics for transistor with TaN gate and HfAlO gate dielectric