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Influences of Ion Implantation Damages on Elevated Source/Drain Formation for Ultra-Thin Body SOI MOSFET

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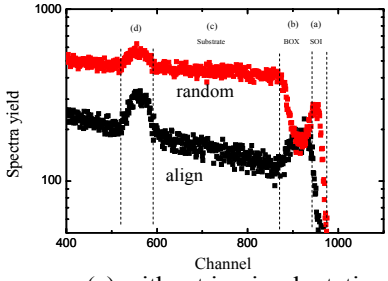
1. Introduction

Ultra-thin body (UTB) SOI CMOS is a promising candidate for a future device with both low-power and high-speed. However, the ultra-thin film layer of UTB SOI CMOS causes a serious disadvantage such as high source/drain (S/D) resistance. Therefore, the elevated S/D (ESD) structure is indispensable to reduce the parasitic S/D resistance [1]. We have fabricated the ESD structure by a selective epitaxial growth (SEG) technique using ultra-high vacuum chemical vapor deposition (UHV-CVD) facility. However, the surface morphology of the grown epitaxial layer is an important for lowering resistance and junction leakage current, which has a tight relationship with the surface state of the top Si layer. Therefore, the SEG process can be influenced by various treatments performed before the UHV-CVD process. For example, it has recently been reported that the damage of top Si layer can be induced by dry etching process used for the fabrication of sidewall spacers [2].

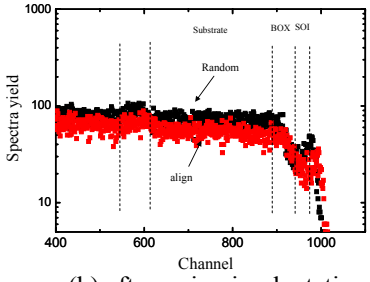
We have been investigated the morphology of the SEG layer on the ultra thin silicon film with and without ion implantation. The ion implantation is widely used to form a SDE and S/D region of MOSFET. However, ion implantation into ultra-thin film SOI presents problems that did not exist in bulk Si. In this work, the morphologies of the SEG layer on the ultra thin silicon film and the crystallinities of the top Si layer are investigated by using FE-SEM and RBS system. Furthermore, a sacrificial sidewall spacer method to suppress the ion implantation damages is proposed and UTB SOI MOSFETs with the elevated S/D having a good surface morphology is evaluated.

2. Crystallinity and roughness of implanted ultra thin SOI film

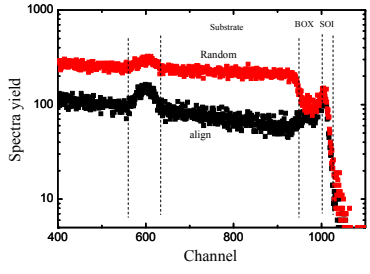
The Si layer damaged after ion implantation is normally recrystallized by thermal process. However, in the case of thin film SOI structure, the recrystallization of amorphous layer may difficult than bulk-Si, since contact area with the seed layer for recrystallization may not sufficient. It is due to the BOX layer under the top Si layer. Experimentally, recrystallization of SOI structure at the same annealing temperature is significantly difficult to achieve the good quality of Si layer as compared with that of bulk Si. Hence, the crystallinity before and after annealing of the implanted SOI was characterized. The crystallinity was measured by rutherford backscattering spectrometry (RBS). The samples were prepared with As^+ ions implantation for $5x10^{14}$ /cm^2 at 10 keV and without implantation, respectively. Figure 1(a) shows the RBS spectra obtained from a SOI sample without ion implantation. Figure 1(b) shows the RBS spectra of as-implanted sample by As^+ ion, 10keV. In this case, the spectrums of aligned and random are coincident. It seems that the as-implanted top Si layer was fully amorphized. Figure 1(c) shows the RBS spectra of annealed sample by rapid thermal anneal (RTA). The spectrum yield of top Si increases to the level of the random yield. Therefore, in the case of thin film SOI, it is found that the implanted top Si thin film is not perfectly recrystallized after RTA. This may be significantly influenced on SEG process.



(a) without ion implantation



(b) after as ion implantation



(c) after RTA of ion implanted SOI

Fig. 1 RBS spectra of top Si with several conditions.

3. Selective epitaxial growth (SEG) for elevated S/D

To investigate the influence of ion implantation on the selective epitaxially growth (SEG) in ultra thin SOI film experimented in detail. First, the thickness of SOI film was

thinned by thermal oxidation and HF wet etching up to ~30nm, followed by patterning the TEOS SiO_2 by ICP-RIE. After that, ion implantation of several conditions was carried out. After then, the SEG process was worked by UHV-CVD after rapid thermal annealing. The influence of ion implantation after SEG process by observation of FE-SEM was found as shown in the Fig 2. It is confirmed that the SEG process on ultra thin Si film has dependence of surface morphology influenced by ion implantation. Cross-sectional FE-SEM images of SEG-Si grown in SiO_2 patterned SOI substrates shows in Fig. 2(a) without ion implantation, Fig. 2(b) with BF_2 ion implantation, and Fig. 2(c) with As^+ ion implantation. It is found that the SEG on ultra thin Si film had bad surface morphology of SEG on ultra thin Si film in case of grown both after BF_2 ion implantation and after As ion implantation. Furthermore, after Ni silicidation on SEG, we measured sheet resistances by 4-point probe. In the figure 3, the sheet resistance shows the dependence on dopants type, since the morphologies of SEG are different as dopants type.

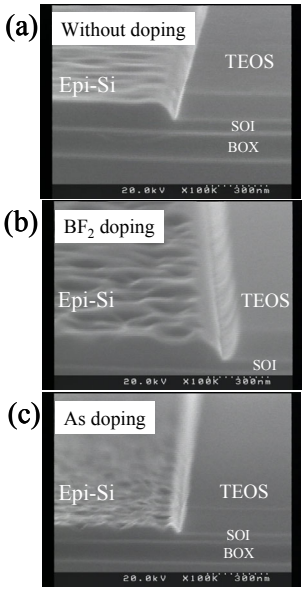


Fig. 2 Cross-sectional FE-SEM images of SEG-Si grown in SiO_2 patterned SOI substrates. (a) without ion implantation, (b) with BF_2 ion implantation ($5\times10^{14}cm^{-2}$, 10keV), (c) with As ion implantation ($5\times10^{14}cm^{-2}$, 10keV) on surface Si of SOI substrates.

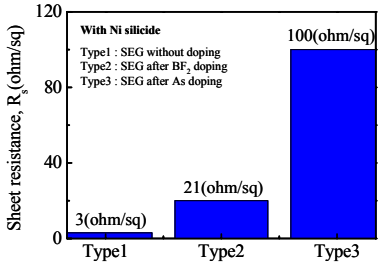


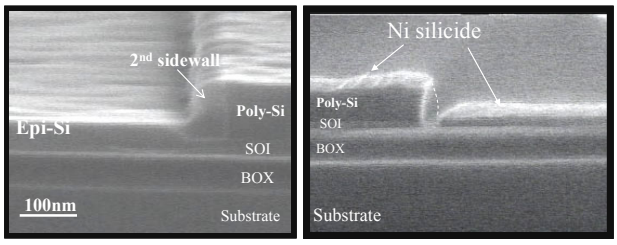
Fig. 3 The sheet resistance of Ni silicide on SEG-Si.

4. Fabrication of ultra-thin body SOI MOSFET

By the results of experiment, it is found that the morphology and roughness of the SEG layer was strongly dependent on the ion implantation damage. So we proposed the advanced SEG formation method with sacrificial sidewall spacer to grow without ion implantation damages.

We have grown SEG-Si without ion implantation damages by using the sacrificial sidewall spacer to grown without ion implantation damages. By using this method, the ultra thin body SOI MOSFET with elevated S/D is fabricated. After the poly-Si gate electrode patterning, 5nm thick TEOS SiO_2, 5nm thick Si_3N_4 film and 70nm thick TEOS SiO_2 is deposited and subsequently, etched to form 80nm sacrificial sidewall spacer. That sidewall spacer is striped by wet etching after SEG-Si.

As shown in Fig. 4, it is observed that the surface morphology of the selective epitaxially grown Si layer was flat and smooth. Figure 4(a) is before Ni silicidation, and figure 4(b) is after Ni silicidation. As results, we could be obtained a good drivability of fabricated SOI MOSFET due to the reduction in the S/D parasitic resistance, as shown in Fig 5.



(a) After SEG (b) After SEG and Ni silicidation

Fig. 4 Cross-sectional SEM images of SEG-Si grown and after Ni silicidation.

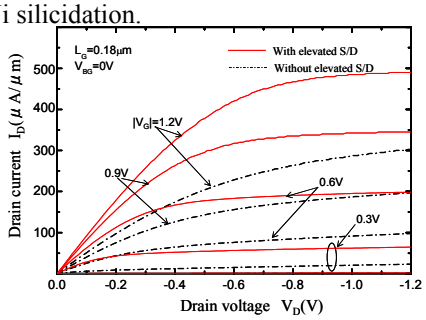


Fig. 5 Drain current characteristics of ultra-thin body SOI PMOSFET.

5. Conclusions

In case of SOI substrate with ultra thin Si film, it is confirmed that the morphology of the selective epitaxially growth (SEG) is strongly dependent on the ion implantation damages. Furthermore, from the RBS measurements, it is found that the implanted top Si of SOI sample after RTA is not perfectly recrystallized. To solve those problems, the sacrificial sidewall process was utilized to form SEG for elevated S/D without ion implantation damages. By this technique, we successfully fabricated the elevated S/D of flat surface ultra-thin body SOI MOSFET with high performance and low sheet resistance of S/D.

References

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