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Ion-Implanted p/n Junction Characteristics in p- and n-type Germanium

T. Nishimura, M. Toyama, K. Kita, K. Kyuno and A. Toriumi

Department of Materials Engineering, School of Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan
Phone: +81-3-5841-7161 E-mail: nishimura@adam.t.u-tokyo.ac.jp

1. Introduction

Recently, germanium (Ge) devices have been proposed as one of the emerging devices in the semiconductor technology roadmap[1], because the low filed mobility in Ge is higher than that in Si[2] and the interface layer formation with high-κ gate insulator is dramatically suppressed[3]. However, Ge has a number of challenges for actual device fabrication. The most serious one is a difficulty of achieving device grade p-n junctions with a good repeatability[4]. This paper reports experimental results to form good p-n junctions in Ge, focusing on the annealing process.

2. Experimental

P-type (Ga-doped) and n-type (Sb-doped) Ge substrates were processed for the formation of p-n diodes and diffused layers. Since relatively stable junction properties have been reported on n-Ge, we processed n-type (111) Ge as well as (100) Ge to extract a possible difference of the junction properties between (100) and (111) Ge. The device structures are schematically shown in **Figure 1**.

300 nm-thick SiO_2 was first deposited on Ge substrates, and then contact holes with 100 μm x 100 μm were formed. The surface cleaning process of Ge is still unclear, and in this work the cleaning process by HCl and buffered HF was employed. Boron and phosphorus ions were implanted at 20 keV with $4x10^{15}$ cm^{-2} thorough 10nm-thick SiO_2 films for achieving the peak concentrations of ~$5x10^{20}$ cm^{-3} and ~10^{21} cm^{-3}, respectively. Then, RTA was performed at 400~700 ºC for 10~300 sec in N_2 ambient with 50 nm-thick SiO_2 capping layer. Then Al was thermally evaporated for electrical contacts on the top and the bottom of Ge.

I-V characteristics of p-n junctions were measured in the range from -0.5V to +0.5V. **Figure 2** shows typical I-V curves for p-n diodes as a parameter of annealing temperature for 10 sec for both B and P ion implanted samples. We discuss the forward and reverse current densities at V=|0.5|V for quantitative discussion in this paper. The sheet resistance was measured in the structure as shown in **Figure 1(b)**.

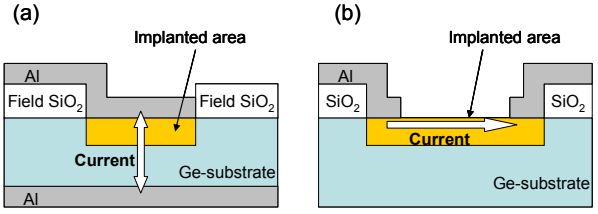

Fig. 1 Schematic illustrations of two kinds of fabricated devices. (a) p-n junction with 100 μm x 100 μm area. (b) Resistor of diffused layer for sheet resistance measurement with 100 μm x 100 μm Al contact area.

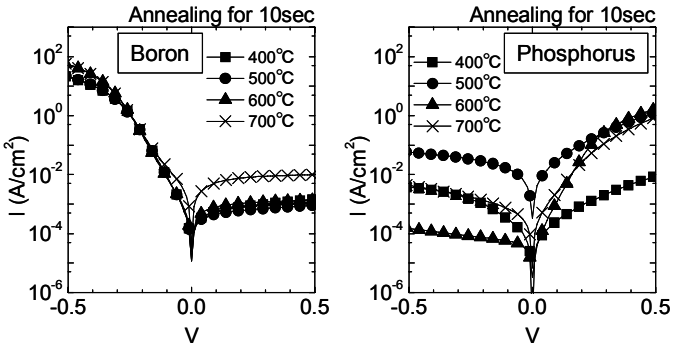

Fig. 2 I-V Characteristics of Ge p^+/n and n^+/p diodes on (100) Ge annealed at various temperature for 10 sec.

3. Results and Discussion

3.1. Boron implanted germanium

Figure 3 shows both forward and reverse currents for three kinds of annealing times as a function of annealing temperature. The forward currents are almost flat with increasing annealing temperature, while the reverse current becomes worse at 700 ºC on (100) Ge. In the case of B implanted p^+/n junctions, the annealing temperature should be lower than 700 ºC so as to obtain diode properties for device application with the junction leakage current around 10^{-3} A/cm^2 and with the forward/reverse current ratio around 10^4.

Both measured and roughly calculated sheet resistances are shown in **Figure 4(a)**, assuming that all implanted ions were electrically active. In **Figure 4(b)**, the ideality factor, *n*, was calculated by averaging the resistance between 0.08 and 0.15 V forward bias regions. *n* is larger than 1.5 in the

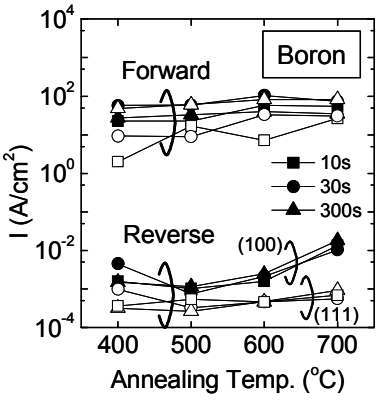

Fig. 3 Forward current versus reverse current of boron implanted p^+/n diodes in various annealing conditions on (100)Ge (solid symbol) and (111)Ge (open symbol) substrates. The annealing time values are varied 10s (■,□), 30s (●,○) and 300s (▲,Δ). Each point is the average of 10 points with a small variation.

case of 700 ºC annealed (100) Ge samples. Since the measured sheet resistance of p^+ layer gradually decreases with annealing temperature increase, those results indicate that the dopant activation is enhanced and the recombination centers are increased with the annealing temperature increase.

In addition, it is interesting to notice that (111) Ge looks more robust against thermal annealing than (100) Ge in terms of p/n junction formation.

3.2. Phosphorous implanted germanium

The case of P is significantly different from that of B. **Figure 5** shows that both forward and reverse currents are affected by the annealing temperature and time. It looks noisy but seems that annealing between 500~600 ºC will be adequate for activating implanted P ions and for annihilating generated defects. The average P concentration is approximately estimated as ~10^{20} cm^{-3}(annealing at 400 ºC for 10s) ~ ~10^{19} cm^{-3}(annealing at 700 ºC for 300s), by calculating annealed profiles by using the diffusion coefficient data[5]. Since the measured sheet resistance is much higher than the calculated one as shown in **Figure 6(a)**, it is inferred that most of the implanted ions are inactivated even by the high temperature annealing. The ideality factor in **Figure 6(b)** is substantially higher than the case in **Figure 4(b)**. Thus, it is concluded that a suitable range for annealing temperature and time for n^+/p junction formation is quite narrow as compared with that for B implanted case.

3.3 Discussion

In the P implanted case, it is expected that a number of inactivated ions still remain in Ge substrates. The maximum equilibrium solid solubility of P in Ge is reported to be 2x10^{20} cm^{-3} at 550 ºC[6]. However, the solubility of P in the present experiment was approximately estimated to be ~10^{19} cm^{-3}. It means that inactive ions can be an origin for the generation-recombination center. Therefore, in order to reduce the reverse leakage current, P concentration in the depletion layer should be substantially lowered and may be profiled like the LDD (lightly doped drain) structure in CMOS.

Another interesting feature is the surface orientation dependence of the reverse leakage currents in the case of B implanted p/n junctions. Now the results are quite phenomenological and further study with more data will be needed to clarify possible origins, including the investigation of both bulk and surface quality of Ge wafers. In the development of Ge device technology, most of the process details quite common to the Si technology should be reconsidered.

4. Conclusions

We have investigated the p-n junction diode on Ge substrates by using B and P ions implantations. The ratio of forward current to reverse one was lager than 10^4 in the case of p^+/n junction, while that was not stable but typically 10^2 in the n^+/p junction. In the case of P implantation, it is recommended that the profiled source and drain formation might be employed.

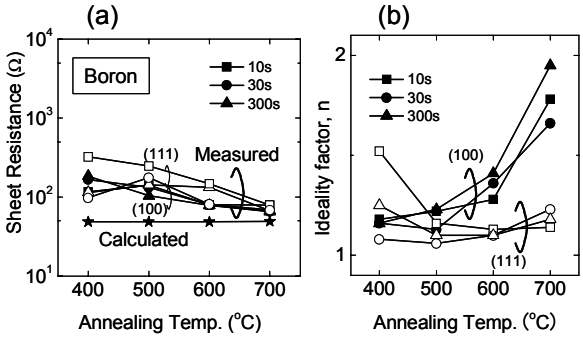

Fig. 4 (a) Measured and calculated sheet resistances for 10s annealing at 400~700 ºC on boron implanted (100) Ge (solid symbol) and (111) Ge (open symbol). (b) Ideality factor obtained between 0.08 and 0.15V for (100), (111) Ge substrates.

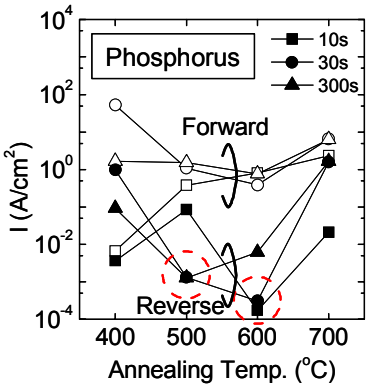

Fig. 5 Forward current (open symbol) versus reverse current (solid symbol) of phosphorus implanted n^+/p diodes in various annealing conditions on (100) Ge. The annealing time values are varied 10s (■,□), 30s (●,○) and 300s (▲,Δ). Each point is the average of 10 points with a small variation.

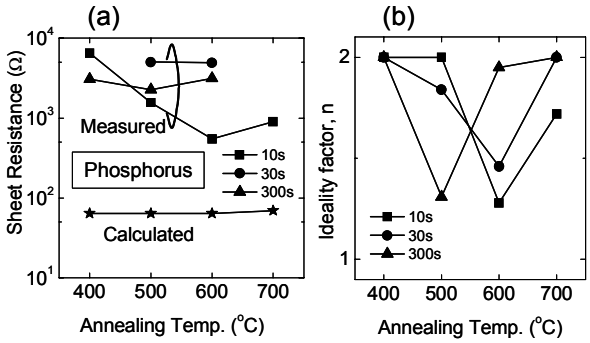

Fig. 6 (a) Measured and calculated sheet resistances for 10s annealing at 400~700 ºC on phosphorus implanted (100) Ge. (b) Ideality factor obtained between 0.08 and 0.15V.

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