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Impact of Annealing Methods and Sequences on Dopant Activation and Diffusion of Ultra-shallow Implanted Silicon

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1. Introduction

For high performance advanced devices with below 65 nm design rules, the formation of abrupt ultra-shallow junctions (USJ) becomes a significant technical challenge. The higher electrical activation of heavily implanted Si without dopant diffusion and residual crystalline damage is one of the principal challenges [1].

The combination of "soak" and "spike" rapid thermal anneal (RTA) are widely used for implant activation applications. The annealing time for typical "soak" anneal is in the range of 10~30 s at a specified temperature. The "spike" annealing duration is typically less than 1.5 s within +/- 50^{o}C from the desired peak temperature. To further improve the dopant activation rate with minimal dopant diffusion, a very rapid surface anneal (<10 ms) at a very high temperature (>1100^{o}C) is considered the most promising solution to maximize electrical activation of dopants without causing diffusion [1, 2].

In this study, $^{11}B^+$ and $^{49}BF_2^+$ implanted Si wafers with various implant energies and doses were annealed to investigate the effect of a novel millisecond flash annealing with or without a combination of conventional RTA on the electrical activation and dopant diffusion.

2. Experiment

Low energy B implanted n-type and p-type silicon wafers with various resistivities were annealed using combinations of a novel millisecond flash anneal and a conventional tungsten halogen lamp-based RTA. Typical implant energies and doses are $^{11}B^+$ 0.5~2.0 keV, 1.0~4.0 x 10^{15} cm^{-2} and $^{49}BF_2^+$ 2.0~5.0 keV, 0.4~1.5 x 10^{15} cm^{-2}. Approximately one half of the wafers were preamorphized by Ge implantation ($^{72}Ge^+$ 5.0~30.0 keV, 0.5~2.0 x 10^{15} cm^{-2}). The duration of the flash was controlled between 1 ms and 20 ms by controlling the flash discharge energy in the range of 0.05 MJ ~ 0.5 MJ. Sheet resistance (Rs) of implanted wafers was measured using a four point probe. The B depth profile was measured using secondary ion mass spectroscopy (SIMS). The junction depth, x_j (at a B concentration of 1.0 x 10^{18} cm^{-3}), movement of implanted wafers after annealing was estimated from the SIMS B depth profiles.

3. Results and Discussions

The as-implanted junction depth of $^{11}B^+$ (1.0 keV, 2.0 x 10^{15} cm^{-2}) implanted wafers with Ge pre-amorphization (5.0 keV, 1.0 x 10^{15} cm^{-2}) was 26.0 nm. The Rs of 460 ohm/sq. is achieved after 100% flash at 400^{o}C without B diffusion. At a pre-heat temperature of 700^{o}C, the Rs of 432 ohm/sq. and x_j increase of 3.5 nm were measured. Significant Rs reduction as well as B diffusion (x_j = 47.0 nm, 21 nm depth increase) were observed at a pre-heat temperature of 800^{o}C. No Ge diffusion was observed at any of the annealing conditions. (Fig. 1 (a) and (b))

The Rs values from $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers with and without Ge pre-amorphization are shown in Fig. 2 as a function of junction depth (x_j) after flash anneal under various conditions. Estimated Rs values of an ideal USJ with a box profile are plotted as a function of carrier concentration and junction depth. The carrier concentration was estimated to be is 1.0~2.0 x 10^{20} cm^{-3} after flash anneal. As flash power increases and effective annealing temperature increases, the enhancement of electrical activation was observed in flash annealed wafers.

The effect of flash anneal on previously "spike" or "soak" annealed wafers ($^{11}B^+$ 2.0 keV, ~4.0 x 10^{15} cm^{-2} on p-type Si) using the conventional RTA systems was investigated to see whether a subsequent flash anneal can provide additional dopant activation [3]. The subsequent flash anneal did not result in additional dopant diffusion. The wafers reprocessed by the flash annealing system showed additional electrical activation without additional B diffusion. The wafers annealed with reverse sequences (flash anneal followed by "soak" or "spike" anneal) showed higher effective level of electrical activation (Rs/x_j) with slightly less B diffusion compared to the wafers where flash followed the anneal. The Rs and x_j values obtained under various combinations of flash anneal and conventional RTA conditions are summarized in Figs. 3 and 4.

4. Summary

Flash anneal of ultra-shallow implants is found to be very effective in forming abrupt ultra-shallow junctions. The combination of flash anneal and conventional RTA are demonstrated to be very effective in controlling both electrical activation and dopant diffusion. The surface annealing using a short wavelength, high power flash is confirmed to be very effective in electrical activation of fast diffusing dopants such as B without significant diffusion. Flash anneal is promising as a shallow junction implant anneal technique for advanced devices with 65 nm node and beyond.

References

[1] W.S. Yoo and K. Kang, Electrochem. Soc. Proc., **PV 2002-14** (2003) 111.
[2] W.S. Yoo and K. Kang, Electrochem. Soc. Proc., **PV 2004-01** (2004) 3.
[3] J. Harnish, C. Carson, J. Foggiato, K. Kang and W.S. Yoo, 207th Electrochem. Soc. Meeting, (2005) to be presented.

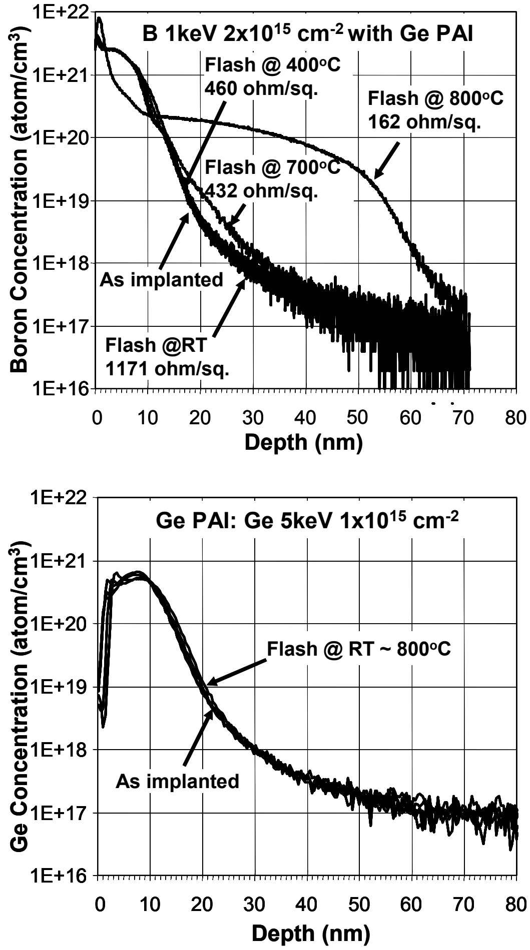

Fig. 1 SIMS depth profiles of B (top) and Ge (bottom) of B 1.0 keV, 2.0 x 10^{15} cm^{-2} before and flash annealing under various conditions.

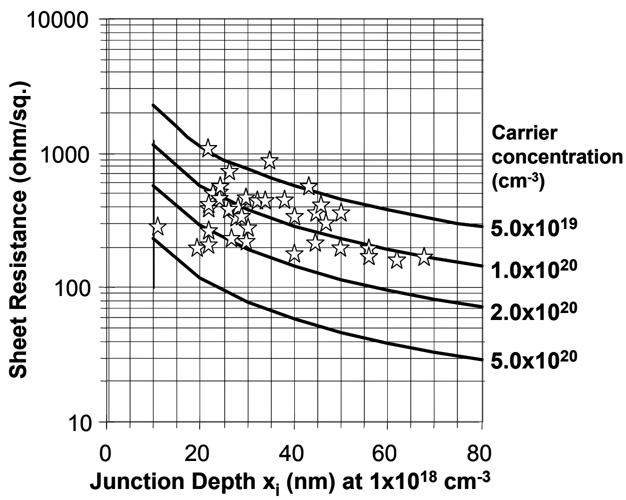

Fig. 2 Rs and x_j values achieved on various ultra-shallow implanted wafers under various flash annealing conditions.

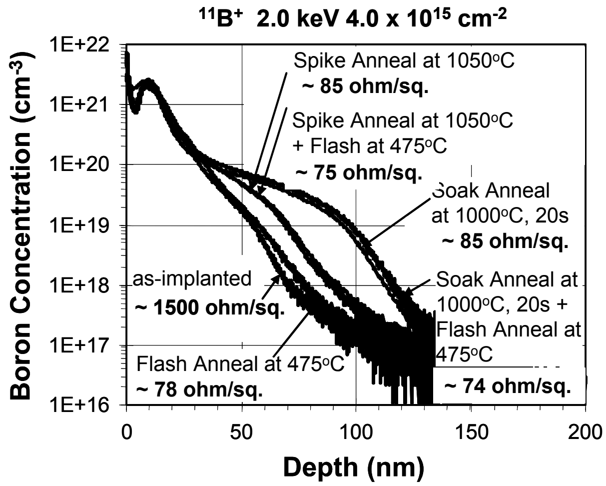

Fig. 3 Typical Rs values and SIMS B depth profiles of as-implanted and wafers annealed under various conditions.

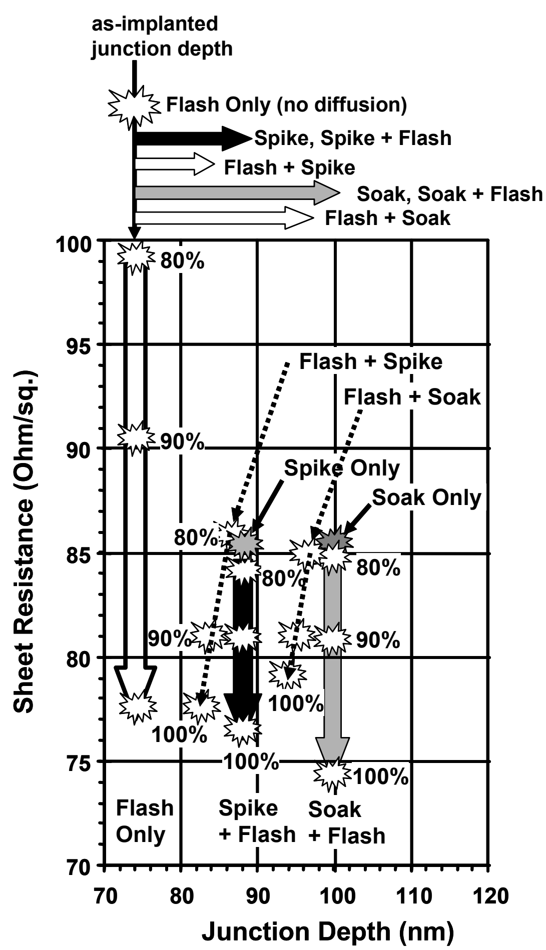

Fig. 4 Rs and x_j plot under various combinations of flash anneal and conventional lamp-based RTA conditions. (Numbers in the figure represent flash power)