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Application of Microwave Plasma Gate Oxidation to Strained-Si on SiGe and SGOI

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1. Introduction

Combining strained-Si MOSFETs with SiGe-on-insulator (SGOI) substrates results in further performance enhancement as demonstrated.[1] One of critical issues in integration of strained-Si devices is oxidation. We have found that surface roughness increases when thermal oxidation is applied to strained-Si/SiGe to form gate oxide due to local inhomogeneity of strain.[2] The increased roughness can cause decrease in channel carrier mobility.

Another issue concerned with oxidation is the formation of Ge condensed layer beneath the oxidation formed SiO_2 layer, which takes place conventional thermal oxidation is applied to SiGe. The Ge condensed layer at the sidewalls of trench isolated active area in strained-Si/SiGe or the sidewalls of the MESA isolated active island in strained-Si/SGOI induces the side channels which significantly degrade the subthreshold characteristic of MOSFET.

In this paper, we show that plasma oxidation, which can perform oxidation at low temperature, can overcome these issues associated with thermal oxidation. The plasma oxidation proceeds under diffusion limited condition and, therefore, it provides strain independent oxidation kinetics and produces smooth gate-oxide interface. Preliminary results of the plasma oxidation was presented in our previous report.[3] This paper reports our new finding that post-plasma-oxidation treatment in wet ambient at low temperature remarkably reduces the oxide interface charge and the mobility enhancement predicted by the theory [4] is achieved. It is also shown that plasma oxidation can suppress the formation of Ge condensed layer and, therefore, the subthreshold characteristic of MOSFET is very much improved.

2. Experimental

The strained-Si/SiGe and strained-Si/SGOI samples were used in this study. The former was used to characterize the gate-oxide interface and the latter was used to investigate the Ge condensation phenomenon at the MESA sidewalls and its effect on the subthreshold characteristic of MOSFET. For the strained-Si/SiGe, a 2 μm-thick graded SiGe layer was first grown on Si (100) followed by the growth of 1 μm-thick $Si_{0.85}Ge_{0.15}$ layer and the growth of 20 nm-thick strained-Si layer. In case of the strained-Si/SGOI, thicknesses of strained-Si, $Si_{0.85}Ge_{0.15}$ and BOX were 16, 70 and 150 nm, respectively. Plasma oxidation was performed at 400°C for 3 hours. 2.45 GHz microwave was applied to excite plasma. No other gas than pure O_2 was supplied. The pressure and the incident microwave power were 0.5 Pa and 100 W, respectively. Post-plasma-oxidation treatment was carried out at 450°C for 60 min in wet-O_2 ambient. Samples whose gate oxide was formed by thermal oxidation at 800°C for 3 hours were also prepared for reference.

3. Results and Discussion

The low-frequency C-V characteristics measured for the plasma gate-oxide of strained-Si/$Si_{0.85}Ge_{0.15}$ MOS capacitor before and low-temperature wet-O_2 treatment are shown in Fig. 1. The C-V curve of the as-grown oxide shows larger shoulder which indicates the presence of a high interface state density. On the other hand, it is clearly shown that the interface characteristics is very much improved by the low-temperature wet-O_2 treatment. The C-V curves indicate the reduction in interface state density in the lower half of the bandgap from 3×10^{12} $cm^{-2}eV^{-1}$ of the as-grown sample to less than 2×10^{11} $cm^{-2}eV^{-1}$ of the wet-O_2 treated sample.

Figure 2 shows field effect mobility μ_{eff}- effective normal field E_{eff} curves obtained for n-channel MOSFETs fabricated on strained-Si/SiGe. The low-temperature wet-O_2 treatment results in the reduction of threshold voltage and the increase in μ_{eff}. In the figure, a curve obtained for a MOSFET fabricated on bulk non-strained-Si wafer is also shown. We find that 60% mobility enhancement is achieved by employing the plasma-oxidation and post-oxidation treatment. Besides, the fact that the μ_{eff} of the plasma-oxidized strained-Si MOSFET is higher than that of the thermal-oxide device at high E_{eff} region suggests that the formation of smoother gate-oxide interface in the plasma-oxide device than in the thermal-oxide device.

In terms of Ge condensation, Fig. 3 shows HAADF-STEM images and EDX profiles for Si and Ge at the MESA sidewalls of 27%-Ge SGOI sample after dry oxidation at 800°C for 3 hours. Formation of a Ge condensed (50% Ge) layer under beneath the 10 nm thick SiO_2 layer is clearly observed.

In the case of plasma oxidation, as can be seen in the AES profiles shown in Fig. 4, no Ge-condensed layer is formed under the surface oxide layer. The oxide layer is composed of SiGe oxide. Figure 5 shows subthreshold characteristics of strained-Si/SGOI MOSFETs fabricated using the dry thermal oxidation and the plasma oxidation followed by wet-O_2 treatment. The results clearly indicate that the formation of the side-channels is suppressed by replacing dry oxidation with plasma oxidation which results in improved subthreshold characteristic.

4. Conclusion

Plasma oxidation in combination with post-oxidation wet-O_2 treatment produces high quality gate oxide in terms of (1) mobility enhancement of strained-Si/SiGe and strained-Si/SGOI, (2) suppressing the formation of the side-channel, and (3) low-temperature processing.

Acknowledgements

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References

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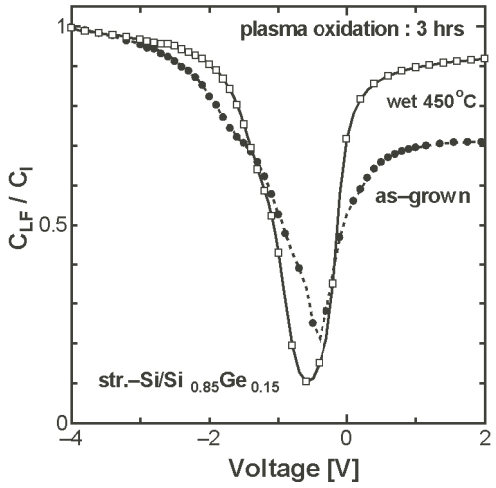

Fig. 1: C-V characteristics of MOS capacitors with as-grown plasma oxide and wet-O_2 treated plasma oxide.

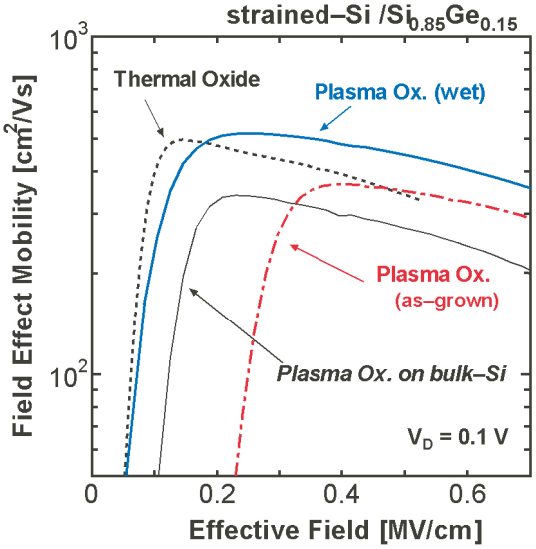

Fig. 2: μ_{eff}-E_{eff} curves of n-ch MOSFETs on strained-Si/SiGe with plasma gate oxide and thermal oxide. The curve obtained from bulk Si control is also shown.

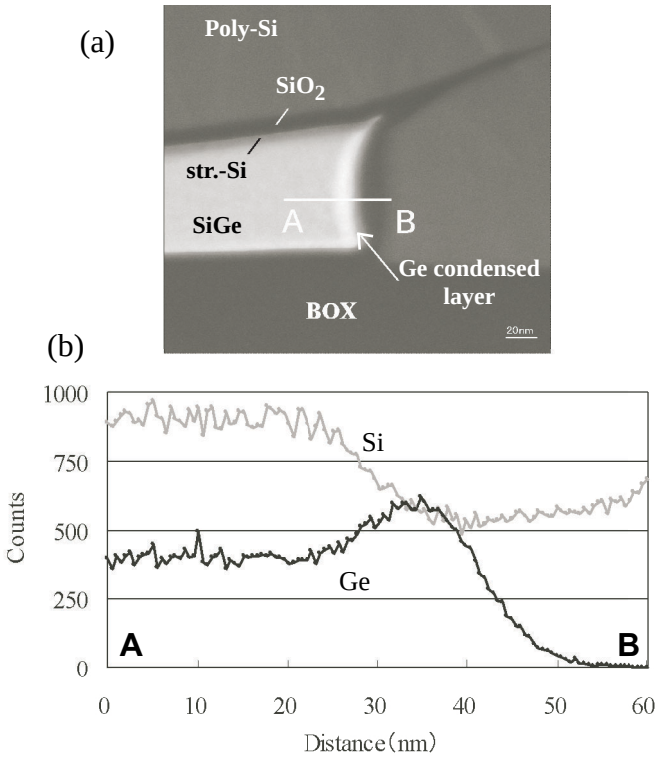

Fig. 3: HAADF-STEM images (a) and EDX profiles (b) at the sidewall of SGOI MESA island after dry oxidation.

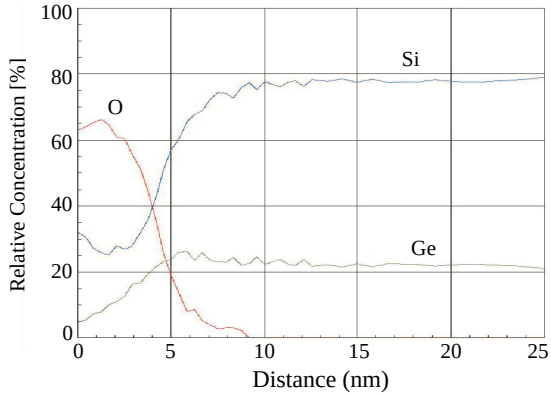

Fig. 4: AES depth profiles for plasma oxidized for SiGe.

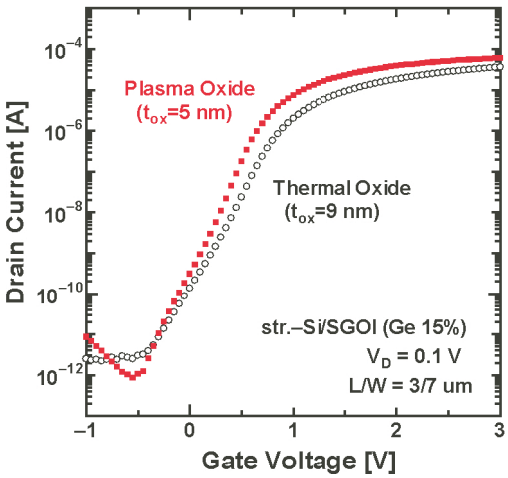

Fig. 5: Subthreshold characteristics of MOSFETs fabricated on str.-Si using plasma oxidation with wet-O_2 treatment and dry oxidation.