P1-25

Damage-Free Microwave-Excited Plasma Contact Hole Etching without Carrier Deactivation at the Interface between Silicide and Heavily-Doped Si

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Introduction

As the size of LSI shrinks, low contact resistivity at the source/drain contact should be needed because the contact resistance is inversely proportional to the contact window area. In particular, parasitic series resistance due to the source contact decreases observed transconductance g_m of MOSFET represented by $g_m = g_{mi} /(1+ R_s \cdot g_{mi})$, where g_{mi} and R_c are the intrinsic transconductance without parasitic series resistance and the source contact resistance respectively. This degradation effect becomes serious as g_{mi} increases. In order to realize low contact resistance, high carrier concentration at the interface between the metal and the heavily-doped Si as well as a low barrier height is essential. However, usual source/drain contact opening processes using the plasma deactivate the carrier due to high-energy ion bombardment and increase the contact resistance. Therefore, plasma etching equipment which can control the ion energy towards the wafer without change in other process parameters such as density of ions or radicals as well as process uniformity is strongly required. The microwave-excited plasma equipment incorporating the dual showerhead structure for SiO_2 contact hole etching[2,3] as well as other etching and PECVD processes can satisfy the above requirements because the etching process region is completely separated from the plasma excitation region. In this article, investigation of carrier concentration at the interface between $TaSi_2$ silicide and heavily-doped Si after plasma irradiation and the application of two-steps damage-free SiO_2 etching technology consisting of high-speed etching mode and damage-free etching mode are described.

Experimental

Fig. 1 shows the microwave-excited plasma etching equipment incorporating the dual showerhead structure for 200mm-diameter wafer. Fig. 2 shows the process flow of fabricating the samples. In-situ consecutive deposition of β-Ta (10nm)/undoped amorphous Si (5nm) by dc sputtering and the two cases of ion mixing implantation of BF_2 (for p+/n junction) and As (for n+/p junciton) were performed[1]. Si capping on Ta realizes oxide-free silicidation. The samples were irradiated by the plasmas (SiO_2 contact hole etching condition) for the cases of (1) $TaSi_2$/n+ or p+-Si and (2) APCVD-SiO_2/ $TaSi_2$/n+ or p+-Si. In the latter case, SiO_2 (500nm) was fully etched. Then, after wet etching of $TaSi_2$, the carrier concentration depth profiles of p+ or n+ Si for the depth range from the silicide interface to few tens of nm depth were obtained by repeating measurement of sheet resistance, anode oxidation using H_3PO_4 and removal of the oxide film.

Results and Discussions

Fig. 3 shows the X-ray diffraction (XRD) spectra for the cases of (a) as-deposited Ta(10nm), (b) BF_2^+ ion implantation on Si/Ta film and (c) annealing of the BF_2^+-ion-mixed Si/Ta film at 550°C for 1 hour. β-Ta becomes amorphous by ion mixing, and successfully transformed to $TaSi_2$ after annealing. Fig, 4 shows the carrier depth profiles of n+/p and p+/n junctions after annealing. The values of carrier concentration at the silicide interface exceed $10^{20}cm^{-3}$, which can realize very low contact resistivity of $\sim 10^{-9}\Omega cm^2$[1]. Fig. 5 shows the carrier depth profile of p+/n junction after irradiation of plasma of $Ar/C_5F_8/O_2$ gas chemistry for the case that self-bias voltages are –230V, -410V and -580V. Initial profiles before the plasma irradiation are also shown. Plasma irradiation time was set to be the ion dose of 5 x $10^{18}cm^{-2}$. Deactivations of the carrier concentration at the interface are found for the self-bias voltages of –410V and -580V, which are adopted values in current contact etching processes. Fig. 6 shows the interface carrier concentration (p+) after the plasma irradiation as a function of self-bias voltage for two gas chemistry cases of $Ar/C_5F_8/O_2$ and $Xe/C_5F_8/O_2$. It is found that the carrier does not deactivate for the self-bias voltage region below ~400V in Xe case, while damages are induced for self-bias voltages larger than ~200V in Ar case. The results suggest that Xe with large atomic radius compared with that of Ar can decrease the damage resulting from the suppression of momentum transfer to the heavily doped Si through the silicide. Fig. 7 shows the SiO_2 etching rate as a function of self-bias voltage for the cases of of $Ar/C_5F_8/O_2$ and $Xe/C_5F_8/O_2$. Damage-free self-bias voltage region for each cases are also indicated. For realization of high through-put in production line, the use of Xe gas has advantage. Fig. 8 shows the carrier concentrations at the silicide interface for two cases of $TaSi_2$/p+/n and $TaSi_2$/n+/p junctions obtained by the application of the two-steps etching of SiO_2 (500nm) on the junctions consisting of high-speed etching mode and damage-free etching mode. The carrier concentration at the interface is plotted as a function of remaining SiO_2 thickness etched by damage-free etching mode. It is found that the damage-free etching can be realized for setting the remaining SiO_2 thickness for damage free etching to be ~100nm.

Conclusion

Damages of carrier deactivation of heavily-doped Si induced by ion bombardment through the $TaSi_2$ induced by contact etching process were investigated. Damages are found at p+ region even by ion-bombardment through the silicide. Two-steps damage-free etching consisting of high-speed etching and damage-free etching is realized using the microwave-excited plasma etching equipment with the dual showerhead structure which can realize uniform processes over large-diameter wafer independent of plasma gas chemistry, working pressure and ion energy towards the wafer (i.e. substrate rf-bias power). Plasma excitation using Xe gas has advantage for realizing both high through-put and damage-free processes. The technology will be a key to realize high-speed analog/digital mixed signal devices.

References

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[2] T. Goto et al., Jpn. J. Appl. Phys. 42 (2003) pp1887-1891
[3] T. Goto et al., Jpn. J. Appl. Phys. Jpn. J. Appl. Phys. 42 (2003) pp. 1884-1887

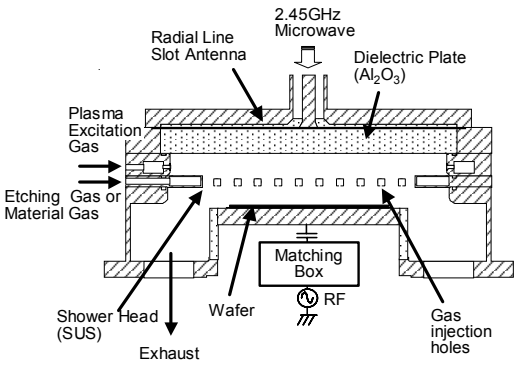

Fig. 1 Schematic view of the microwave-excited plasma etching equipment incorporating the dual showerhead structure.

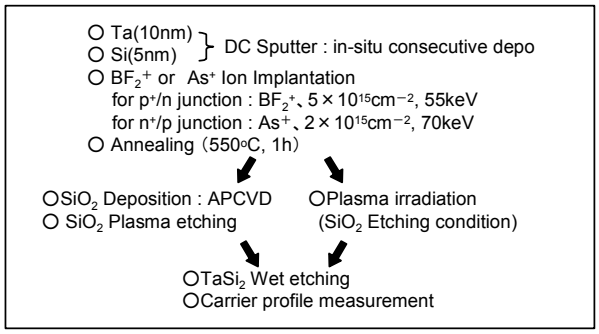

Fig. 2 The process flow of fabricating the samples for damage investigation.

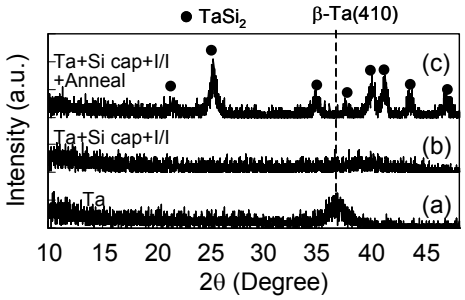

Fig. 3 The X-ray diffraction (XRD) spectra for the cases of (a) as-deposited Ta(10nm), (b) BF_2 ion implantation on Si/Ta film and (c) annealing of the BF_2-ion-mixed Si/Ta film at 550℃ for 1 hour.

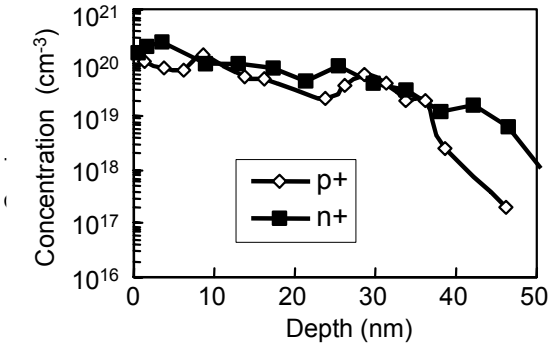

Fig. 4 The carrier depth profiles of n+/p and p+/n junctions after annealing at 550℃ for 1 hour. The values of carrier concentration at the silicide interface exceed $10^{20}cm^{-3}$, which can realize very low contact resistivity of ~$10^{-9}\Omega\cdot cm^2$.

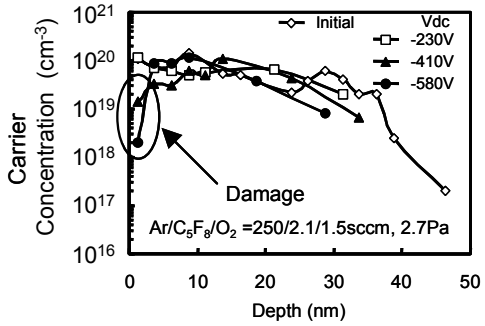

Fig. 5 The carrier depth profile of p+/n junction after irradiation of plasma of $Ar/C_5F_8/O_2$ for some self-bias voltages. Damages are found at the usual self-bias voltage region (-410V, -580V) in current contact etching processes.

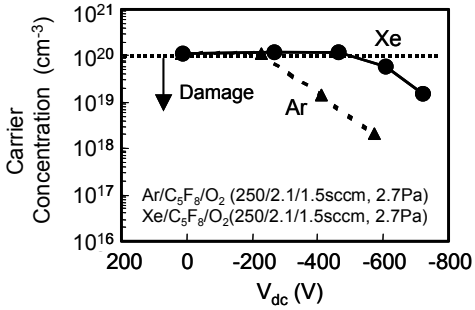

Fig. 6 The interface carrier concentration (p+) after the plasma irradiation as a function of self-bias voltage. Xe with large atomic radius compared with that of Ar can decrease the damage for large self-bias voltage region.

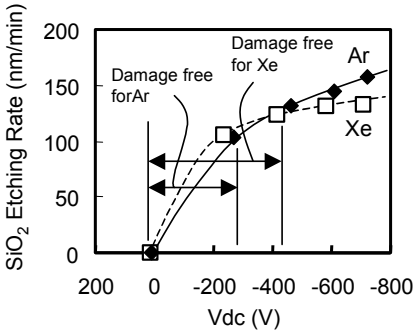

Fig.7 SiO_2 etching rate as a function of self-bias voltage for the cases of of Ar/ C_5F_8/O_2 and Xe/ C_5F_8/O_2. The use of Xe has advantageous for high through-put processes.

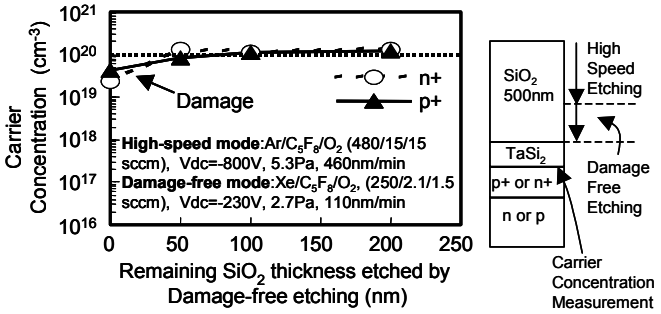

Fig. 8 The carrier concentrations at the silicide interface for two cases of $TaSi_2$/p+/n and $TaSi_2$/n+/p junctions obtained by the application of the two-steps etching of SiO_2 (500nm) on the junctions consisting of high-speed etching mode and damage-free etching mode. The carrier concentration at the interface is plotted as a function of remaining SiO_2 thickness etched by damage-free etching mode. Damage-free etching can realize for setting the remaining SiO_2 thickness for damage free etching to be ~100nm.