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A Novel Explanation of Substrate Bias Dependent Dielectric Breakdown Behavior with Channel Quantization Effect in Ultrathin Oxide pMOSFETs

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ABSTRACT

A new explanation of ultrathin gate oxide (1.6 nm) pMOSFET's substrate bias dependent dielectric breakdown behavior with channel quantization effect is presented. A significant degradation in lifetime induced by a positive substrate bias and a decrease in the power law exponent (n) were observed. The quantitative hydrogen-based model is used to explain this observation while taking the channel quantization effect into consideration. The degradation is attributed to the channel hole quantization enhanced dissipation energy of injected electrons at the anode interface. Using this model, the stress voltage dependence of Time Dependent Dielectric Breakdown (TDDB) in our experiment fit well with simulation results.

Keywords: TDDB, channel quantization, quantitative hydrogen-based model, ultrathin oxide pMOSFETs.

INTRODUCTION

Gate oxide breakdown is considered one of the most important issues in the aggressive scaling-down of oxide thickness. In ultrathin gate oxide devices, high fields applied to oxides result in bulk defect generation, interface state formation, and eventually breakdown. The most widely accepted theories to address the defect generation are the anode hole injection (AHI) model [1] and the anode hydrogen release (AHR) model [2]. However, neither AHI nor AHR can explain the recent observations of voltage-dependent voltage acceleration of oxide breakdown for ultrathin oxides. Accordingly, a power-law extrapolation with a quantitative hydrogen-based model for the degradation and breakdown of ultrathin gate oxides is proposed [3,4]. It has been shown that this quantitative hydrogen-based model can successfully explain the Decoupled Plasma Nitridation (DPN) pressure dependence of oxide breakdown behavior in ultrathin oxide pMOSFETs [5].

Although the substrate bias dependence of oxide breakdown has been discovered in Ref. [6], the lifetime versus applied gate bias characteristics could not be precisely explained by the Vb induced high impact ionization rate at substrate bulk. Besides, the substrate bias dependence of breakdown progression has been presented in Ref. [7]. However, the pre-breakdown behavior was not discussed in it. In this paper, we further discuss the Time Dependent Dielectric Breakdown (TDDB) behavior of ultrathin oxide pMOSFETs biased in inversion under various reverse substrate biases. A significant decrease of power-law exponent induced by substrate bias will be shown. Finally, a modified quantitative hydrogen-based model with channel quantization effect and its simulation results are used to explain these observations.

EXPERIMENTAL

The p+ poly gate pMOSFETs used in this work were fabricated with a 90nm standard CMOS process on n-type silicon substrate. The gate length is 0.09μm, the gate width is 10μm and the physical oxide thickness is 1.6nm. The nitrided gate oxide was grown with UMC standard Decoupled Plasma Nitridation (DPN) process. All devices were stressed using constant voltage stress (CVS) at 140^{0}C. The initial breakdown event (20% current jump in gate current) was defined as oxide breakdown regardless of soft or hard breakdown. The sample size was about 20 ~ 30 samples per stress voltage.

RESULTS AND DISCUSSION

In order to investigate the role of substrate bias in time dependent dielectric breakdown, we simply stressed the devices under various Vb. The results are shown in **Fig. 1.** Apparently, a reverse substrate bias aggravates defect generation and consequently decreases the time to breakdown. Furthermore, the stress voltage dependence of breakdown lifetime was depicted in **Fig. 2.** The stress gate bias varies from –2.5V to –2.9V. We clearly see a decrease of the power law exponent (n) as Vb increases when the power law model was used. This decreases the TDDB lifetime at operating voltage, which is extrapolated from the TDDB lifetime under stress voltage, for some applications under reverse substrate bias.

It was proposed that the decrease of T_{BD} and voltage acceleration factor might be due to the additional impact ionization at the substrate bulk with reverse Vb [6]. However, our works showed that the anode hot hole induced oxide breakdown from substrate impact ionization has an opposite trend with what we have seen in Fig. 2. In **Fig. 3.**, the impact ionization substrate current was used to represent hole generation rate. The junction leakage current between Drain (or Source) and Bulk has been eliminated. 1/Ib, which is proportional to T_{BD}, showed a larger Vg dependence with higher substrate bias. It suggests that the degradation of voltage acceleration factor could not be well explained by this conventional model.

According to the above result, a quantitative hydrogen-based model incorporating channel quantization was proposed to explain the phenomenon. The model is based on two processes related to chemical reactions involving protons [3]. Firstly, electrons, which are injected from the p+ poly gate in the direct tunneling regime, dissipate energy at the anode Si/SiO2 interface and release protons (H^+) from interface suboxide bands, $\xi_1(V,T)$. Secondly, the released protons react with oxygen vacancies (Si-Si), $\xi_2(V,T)$.

$$\xi_1(V,T) = \frac{K_1}{1+\exp((E_{th1}+q\phi_B-qV)/E_o)} \qquad \textbf{Eq. (1)}$$

$$\xi_2(V,T) = K_2 V^2 \exp\left(-\frac{B}{V}\right) \;;\; B = \frac{4(2m_H)^{1/2} t_{ox} E_{th2}^{3/2}}{3q\hbar} \qquad \textbf{Eq. (2)}$$

Where V refers to the electron dissipation energy and the other parameters have the same definitions as in Ref. [5]. The total defect generation rate is given by $1/\xi=1/\xi_1+1/\xi_2$, and the bottleneck for the whole process is the slowest reaction. A detailed explanation of this quantitative hydrogen-based model is described in Ref. [5].Taking the channel hole quantization effect into consideration, the energy band diagram and the dissipation energy of valance band tunneling electrons at the anode Si/SiO2 interface are illustrated in **Fig. 4.** A larger positive substrate bias results in more serious channel quantization and hence the 1st hole subband energy at the channel region increases.

The maximum available energy (E_{max}) is defined as the energy of electrons at the oxide/anode interface as measured with respect to either the anode conduction band or the anode valance band, depending on the availability of empty states in the silicon substrate valance band [8]. Under ballistic direct tunneling injection, $E_{max} = V_{ox} + E_{h1}$ for pMOSFETs stressed in inversion mode, where V_{ox} is the oxide voltage and E_{h1} is the 1st subband energy of channel holes (Fig. 4), while channel holes are mainly distributed at the 1st subband at temperatures under 140^{o}C [7]. **Fig. 5** shows the simulated E_{h1} versus Vg characteristic curve for various substrate biases.

Replacing the V value of Eq. (1) and Eq. (2) by $V \sim E_{max} = V_{ox} + E_{h1}$, the experimental breakdown data fit very well, as shown in **Fig. 6.** The other model parameters obtained from the fit are E_{th1} = 1.8eV, E_{th2} = 0.2eV, E_o = 0.07eV, B = 100V, and $K_1/K_2 = 0.04V^{-2}$. These values are all the same as those in Ref. [3]. This gives an important piece of support to our model. It implies that the decrease of the power law exponent under reverse substrate bias for pMOSFETs stressed in inversion might be due to the variation of the 1st hole

subband energy, which is related to the electron dissipation energy at the anode interface.

CONCLUSIONS

A significant degradation of TDDB lifetime and its voltage acceleration factor by applying a reverse substrate bias was shown in this paper. We discovered that the conventional model, in which substrate bias only influence the impact ionization at substrate bulk, could not demonstrate this phenomenon. Accordingly, a quantitative hydrogen-based model incorporating the channel hole quantization effect is presented to explain this breakdown behavior. Using this model, the simulations results are in agreement with the experiments. The excellent agreement between the model and the experimental data suggests that the lifetime degradation under reverse Vb might be due to the channel-quantization-enhanced electron dissipation energy, which is the energy supply of defect generation, at the anode interface.

FIGURES

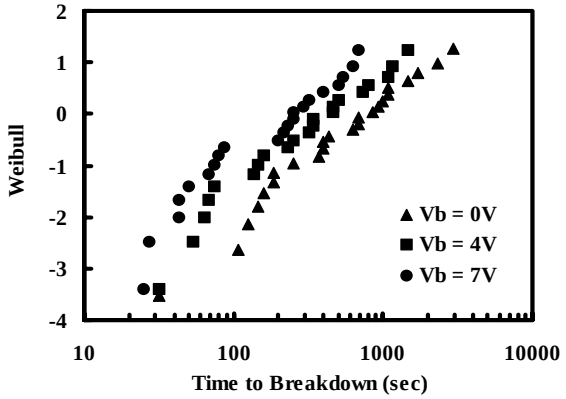

Fig. 1 Weibull distribution of time to breakdown (T_{BD}) on pMOSFETs. The stress gate bias is -2.9V with Vb=0V, 4V, and 7V respectively.

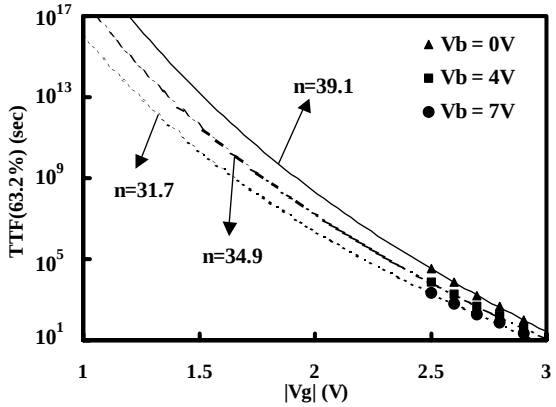

Fig. 2 Stress gate bias dependence of TDDB lifetime. The symbols are experimental data and the curves are extrapolated by the power law model.

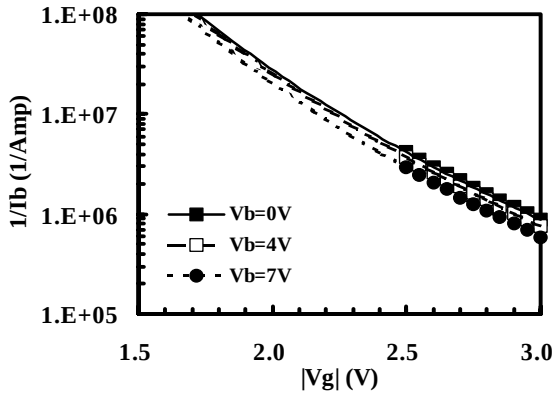

Fig. 3 1/Ib versus gate bias with Vb=0V, 4V, and 7V

REFERENCES

[1] I. Chen, *Appl. Phys. Lett.* vol. 49, p. 669, 1986.
[2] D. DiMaria, *J. Appl. Phys.* vol. 73, p. 3367, 1993.
[3] J. Sune and E. Wu, *VLSI Tech. Dig.*, p. 97, 2001.
[4] E. Y. Wu, et. al, *IEDM Tech. Dig.*, p. 541, 2000.
[5] Ting-Kou Kang, et. al, *IRPS*, p. 596, 2005
[6] J.D. Bude. et. al, *IEDM Tech. Dig.*, p. 179, 1998.
[7] C.W. Tsai, et. al, ***IEEE EDL***, vol. 24, no. 4, p. 269, APR. 2003.
[8] E. Wu et. al, *IEEE EDL*, vol. 23, p. 494, 2002.

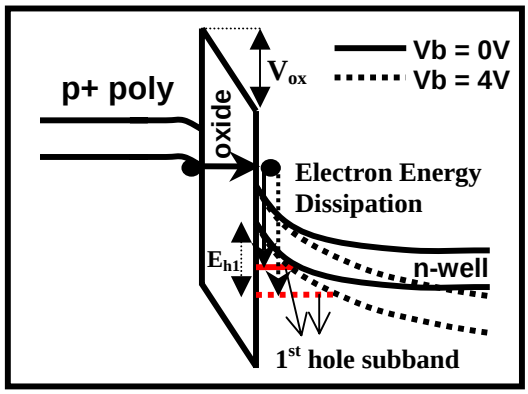

Fig. 4 Illustration of band diagram showing the electron dissipation energy at the anode interface with/without a reverse substrate bias. The electrons dissipate more energy when V_b=4V.

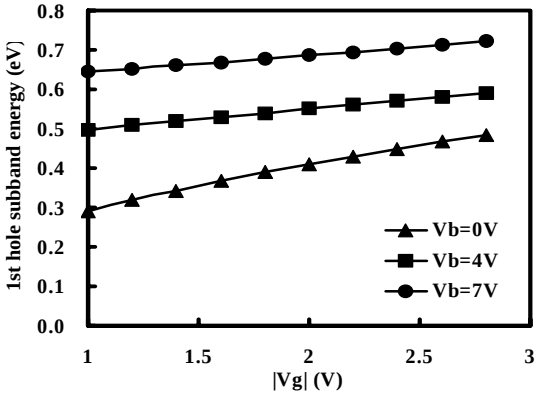

Fig. 5 Simulation of 1st subband channel hole energy at various Vg with Vb=0V, 4V, and 7V.

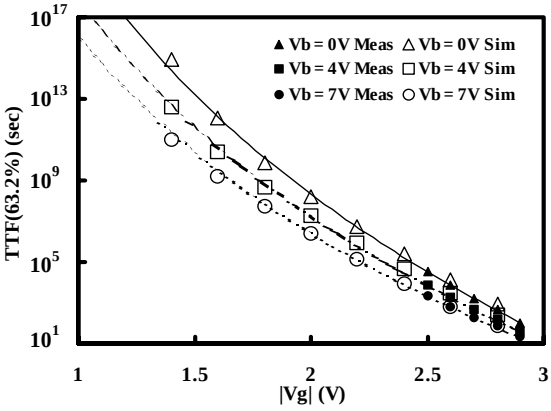

Fig. 6 Lifetime versus Vg plot of measurement and simulation data with various substrate biases.