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Improving high-κ gate dielectrics properties by high pressure water vapor annealing

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INTRODUCTION

Much attention has focused on improving high quality high-κ gate oxides for ULSI applications. High pressure hydrogen anneals have reported to be effective to improve high-κ film interface quality. [1] However, the defects in high-κ gate oxides are distributed across the films, which is different from SiO_2 gate oxide. [2] Therefore, the method to decrease defect bonds of high-κ films is important and selected for this study. Previously, water vapor annealing had been reported as the effective method to improve SiO_2 film quality. [3] This process provides the advantages of low processing temperature, simple, and compatible with ULSI process. We have found that high pressure vapor anneal is effective to improve high-κ gate oxide qualities.

EXPERIMENT

High-κ hafnium silicate ($HfSi_xO_y$) films with a thickness of 9.2 nm were deposited by polyatomic layer CVD (PL-CVD).[4] After the deposition of the films, high pressure H_2O vapor anneal was performed at 260°C with 1.3 MPa steam pressure for different durations. After the treatment, MOS capacitors were fabricated using aluminum electrode for the electrical measurement.

RESULTS AND DISCUSSION

The electrical and physical studies of high-κ films treated with high pressure H_2O vapor annealing were examined. Fig. 1 shows the comparison of leakage current density before and after vapor anneal. Two magnitudes lower in leakage current density and higher breakdown field were observed after short time vapor anneal. Moreover, we have observed that the $HfSi_xO_y$ gate oxides before and after H_2O vapor anneal have different charge transport mechanisms. Fig. 2 shows the I-V characteristics measured at different temperature of the films before anneal. The currents depend strongly on temperature which indicates the dominating Poole Frenkel current transport mechanism. However, the current densities of the films after vapor anneal show less dependent with temperature, as shown in Fig.3. This indicates that Fowler-Nordheim (FN) tunnel is the main charge transport in the annealed samples. This result points toward that trapped sites are decreased by vapor annealing. FN tunneling plot of $HfSi_xO_yN_z$ samples is shown in Fig. 4. The m^*/m^o was assumed to be 0.1. Therefore, the calculated barrier height (ϕ_b) of $HfSi_xO_y$ gate oxide was found to be 1.42 eV. Fig. 5 shows C-V of the samples at different annealing duration. Short time (t<30 minutes) vapor anneal increased the capacitance density but the capacitance decreased when the annealing time was longer than 30 minutes. Comparison of dielectric constant at different annealing durations is shown in Fig. 6.

TEM analysis reveals no significant increase in interfacial SiO_2 layer, as shown in Fig. 7. From FT-IR, we found that Si-O and Hf-O bonds increase after vapor annealing, as shown in Figs. 8 and 9. Therefore, the improvement of electrical properties is due to annihilation of defects by vapor anneal. Fig. 10 shows the proposed model to explain the effect of vapor anneals to reduce the defect bonds by active oxygen and hydrogen species in the case of short time anneals. However, long time anneals introduce the excess –OH bonds which are the source of charge trapping sites.

CONCLUSIONS

The effect of high pressure H_2O vapor anneal was found to improve high-κ film qualities. The active species in the high pressure vapor decreased defect bonds in the bulk high-κ films at annealing duration shorter than 30 minutes. This low temperature annealing method is simple and compatible with ULSI process. This method is effective for the improvement of high-κ film qualities.

REFERENCE

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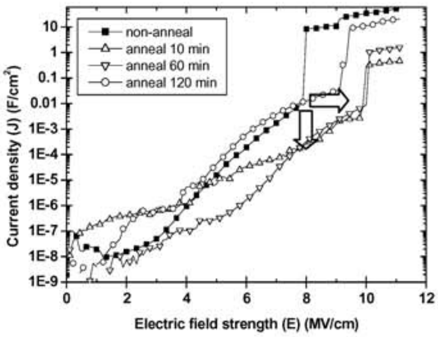

Fig. 1) I-V of $HfSi_xO_y$ films before and after vapor annealing.

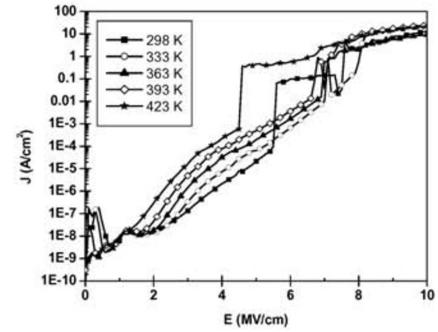

Fig. 2) I-V measured at different temp. of $HfSi_xO_y$ films before vapor annealing.

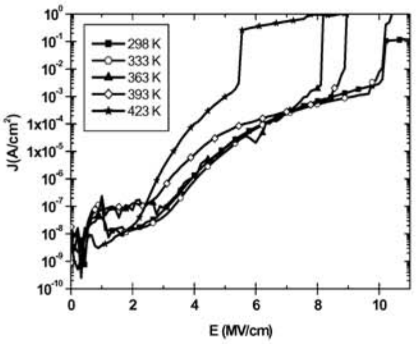

Fig.3) I-V measured at different temp. of $HfSi_xO_y$ films after vapor annealing.

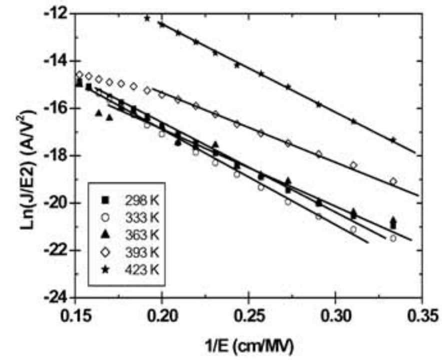

Fig. 4) FN plot of $HfSi_xO_y$ films after annealing measured at different temp.

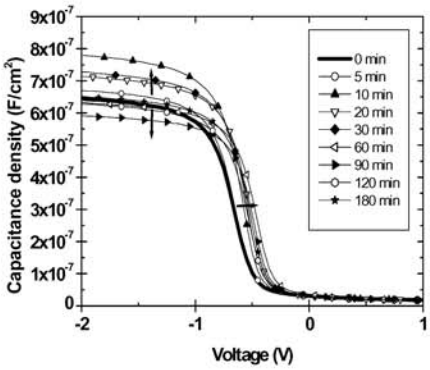

Fig. 5) C-V of $HfSi_xO_y$ films before and after annealing at different time.

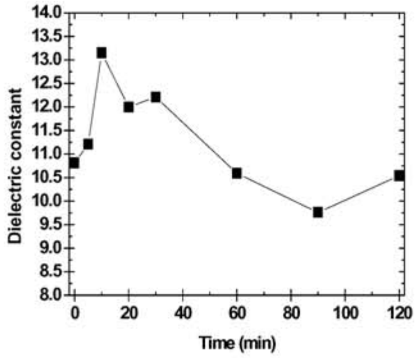

Fig. 6) Dielectric constant of $HfSi_xO_y$ films at different annealing time.

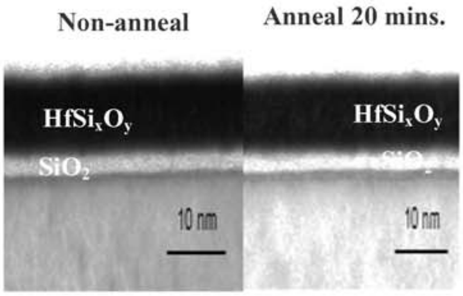

Fig. 7) TEM of $HfSi_xO_y$ films before and after vapor annealing.

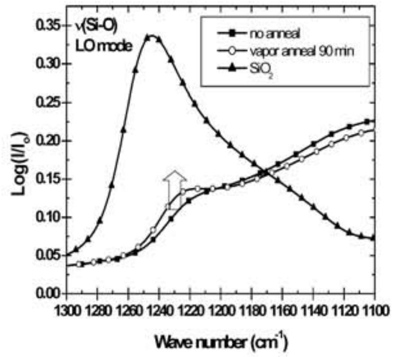

Fig. 8) Comparing Si-O stretching bond before and after vapor annealing.

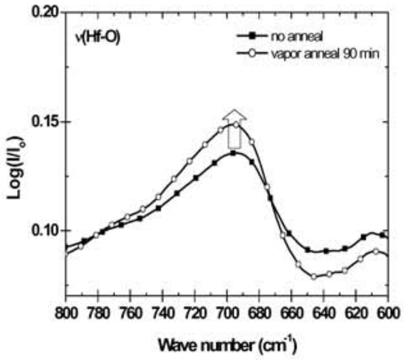

Fig. 9) Comparing Hf-O stretching bond before and after annealing.

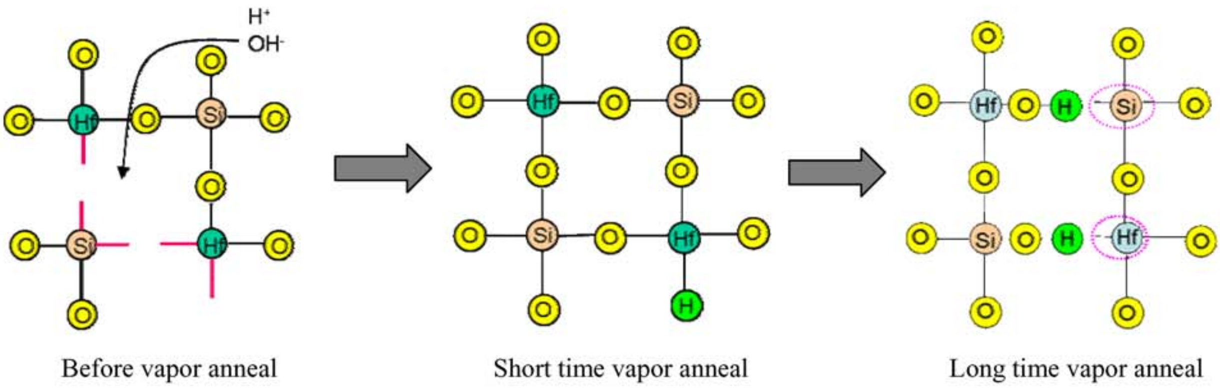

Fig. 10) Model explaining effect of vapor anneal on fixing defect bond in bulk high-κ $HfSi_xO_y$ films.