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Reduction of Accumulation Thickness in Metal Gate

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Abstract
Although it has been believed that highly doped polygate can hardly be accumulated, we will show a decisive evidence for existence of the gate accumulation that contributes to 4Å (nMOSFET) and 3Å (pMOSFET) in accumulation thickness with regardless of gate oxide thickness. This makes an accumulation thickness smaller in metal gate than in polygate.

Introduction
It has been considered that metal gate is necessary to improve transistor performance in 45nm generation and beyond [1-4], since gate depletion width can be excluded from inversion thickness (Tinv) in polygate MOSFETs. On the other hand, there are few reports explaining an accumulation thickness (Tacc) in metal gate is smaller than in polygate, which is clearly seen in the measured CV characteristics [1, 3, 4], since Tacc has been regarded to be same between in polygate and metal gate. We pointed out an importance of the gate accumulation that is due to quantum repulsion effect (QRE) in the analysis of gate capacitance [5, 6]. Here we investigate the gate accumulation in both experimental and theoretical manners, taking into account the QRE. Consequently, it is found that Tacc is thicker by 4Å (nMOSFET) and 3Å (pMOSFET) in polygate than in metal gate.

Experiments
To investigate the gate accumulation, we compare CV characteristics between in polygate and in metal gate. A Ni full silicide (FUSI) gate is fabricated as a metal gate using the process described in Fig. 1. The polygate is obtained if the Ni layer is thinner. Since gate oxides in samples of both gates are prepared with the same oxidation process, the thicknesses of both gate oxides are same. The TEM image of the FUSI gate is shown in Fig. 2. The total flow of the present work is schemed in Fig. 3. The CV-fitting of polygate is carried out to extract the substrate impurity concentration (N_{SUB}) and the oxide thickness (T_{OX}). The CV-fitting of FUSI gate is subsequently carried out using these T_{OX} and N_{SUB} to extract the work function (Φ_{WF}). Here note T_{OX} is used instead of Tacc and Tinv in the present CV-fitting in which the QRE is included.

Theory
Fig. 4 describes an origin of the gate accumulation in polygate while a gate voltage (V_G) is negative. In the left-hand side, the QRE sweeps electrons away from the bended band at the poly-Si surface, since the bended area is too narrow for electrons to be confined there. In other words, the electrons are excited up to 3-dimensional conduction band at the poly-Si surface. The energy levels measured from the conduction band edge at the poly-Si surface accordingly become larger by the band-bending (ΔE). The density-of-states (DOS) is therefore increased in a square-root manner of ΔE. This square-root increase of DOS (δDOS) causes the electron density to be increased at the poly-Si surface, while the DOS is not increased at the metal gate surface. Therefore, this δDOS distinguishes between the polygate and the metal gate. Fig. 5(a) shows the calculation results of carrier densities in a negative V_G. The gate accumulation is clearly shown at the poly-Si surface as the increase of electron density due to δDOS. On the other hand, Fig. 5(b) exhibits the gate depletion as the decrease of electron density at the poly-Si surface. The width of this decreased area turns out almost same as that of the increased area of gate accumulation shown in Fig. 5(a). All the calculations performed here

include the effects of not only the QRE but also incomplete depletion of polygate, subbands of electrons and holes, incomplete ionization and band-gap narrowing [5-7], which results in T_{OX}=Tacc=Tinv. For simplicity, we neglect interfacial transition (IFT) layers [6] from both sides of SiO_2 since a chemical transition in the SiO_2/FUSI interface is unknown and T_{OX} estimated in CV-fitting is irrespective of whether or not the IFT layers are considered, as shown in Fig. 7(a)-(c) of [6]. A quantum-mechanical depletion caused by reflection of wavefunction from an abrupt barrier at the flat band, so-called dark space effect [8], is also neglected. This effect might appear in the gate accumulation, since a wavefunction in the 3-dimensional conduction band to which electrons are excited up by the QRE is similar to the wavefunction at the flat band. As shown in Fig. 6, the gate capacitance is composed of the gate accumulation capacitance (C_{GA}), the oxide capacitance (C_{OX}) and the silicon accumulation capacitance (C_{ACC}) in a negative V_G, while it is composed of the gate depletion capacitance (C_{GD}), C_{OX}, and the silicon inversion capacitance (C_{INV}) in a positive V_G. The C_{GA} as well as C_{GD} are excluded from in metal gate.

Results and Discussion
Shown is the main result of nMOSFETs in Fig. 7. We have obtained excellent agreements between measured and calculated CV characteristics in each gate in both polarities of V_G with regardless of T_{OX}. There are clear discrepancies between polygate and FUSI gate in both polarities of V_G, which means that the gate accumulation as well as the gate depletion exists in the polygate. These discrepancies are compensated in both polarities of V_G with regardless of T_{OX} if T_{OX} is reduced by 4Å in the polygate, which means that the effective thickness (ΔT_{OX}) of gate accumulation is same as that of gate depletion and is estimated 4Å with regardless of T_{OX}. In pMOSFETs, ΔT_{OX} of both gate depletion and gate accumulation are 3Å with regardless of T_{OX}. Fig. 8 shows the ratio of ΔT_{OX} to T_{OX} is then increased as T_{OX} is reduced. The Φ_{WF} of FUSI gate is 4.5eV in nMOSFETs and 4.4eV in pMOSFETs with regardless of T_{OX}. The parameters extracted here are summarized in Table. 1. Discrepancies left between the calculated and measured capacitance in FUSI gate near ±1V, as shown in Fig. 7, can be ascribed to the IFT layers since the dark space effect is most remarkable at the flat band (–0.6V in FUSI gate) [8]. No discrepancy at the flat band suggests that the measured samples include the SiO_2/FUSI IFT layer that breaks the condition of the abrupt barrier for the dark space effect.

Summary
The QRE is necessary to precisely predict the CV characteristics of both polygate and metal gate in both polarities of V_G with regardless of T_{OX}. The ΔT_{OX} is 4Å in nMOSFET and 3Å in pMOSFET with regardless of T_{OX}, which reaches 30-40% at T_{OX}= 1nm. The influence of IFT layer at the FUSI gate interface is left in the CV characteristics, whereas the dark space effect is removed by the IFT layer.

References
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[3] T. Aoyama et al., IEDM04, p. 95 (2004)
[4] K. Manabe, et al., SSDM04, p. 18 (2004)
[5] H. Watanabe, K. Uchida, and A. Kinoshita, SSDM03, p. 270 (2003)
[6] H. Watanabe, D. Matsushita, and K. Muraoka, SSDM04, p. 732 (2004)
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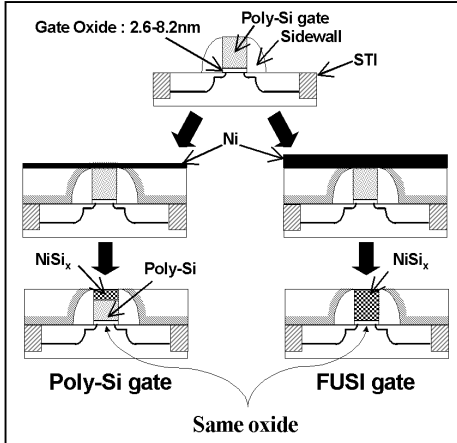[8] A. S. Spinelli, A. Pacelli, and A. L. Lacaita, IEEE TED **47**, 2366 (2000)

Gate Oxide : 2.6-8.2nm
Poly-Si gate
Sidewall
STI
Ni
NiSi$_x$
Poly-Si
NiSi$_x$
Poly-Si gate
FUSI gate
Same oxide

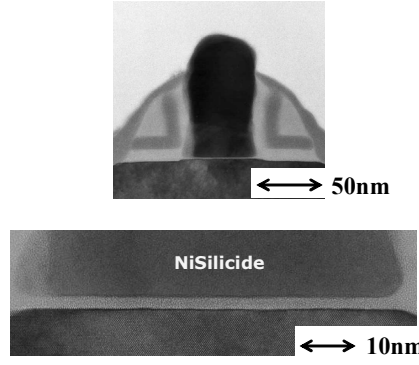Fig. 1 Process flow of sample preparation

50nm
NiSilicide
10nm

Fig. 2 TEM images of FUSI gate

- **Preparation of samples**
- **Measurement of CV characteristics**
- **CV fitting of polygate MOSFETs**
  - extracted
- **Obtaining T$_{OX}$ & N$_{SUB}$**
  - substituted
- **CV fitting of FUSI gate MOSFETs**
- **Obtaining Φ_{WF}**

Fig. 3 Total flow of the present work

$$\delta DOS \equiv \sqrt{DOS_{Surface}^2 - DOS_{Bulk}^2} \approx 6 \times \frac{\sqrt{2}}{\pi^2} \frac{\sqrt{\Delta E}}{\hbar^3} m_{de}^{1.5}$$

Weak accumulation

$$DOS_{Surface} = 6 \frac{\sqrt{2}}{\pi^2} \frac{\sqrt{E - E_C + \Delta E}}{\hbar^3} m_{de}^{1.5}$$

$$DOS_{Bulk} = 6 \frac{\sqrt{2}}{\pi^2} \frac{\sqrt{E - E_C}}{\hbar^3} m_{de}^{1.5}$$

ϕ_{WF}

ΔE

Sweep out of electrons

E_F
E_C
E_V

Band bending

n$^+$poly-Si

Gate Oxide

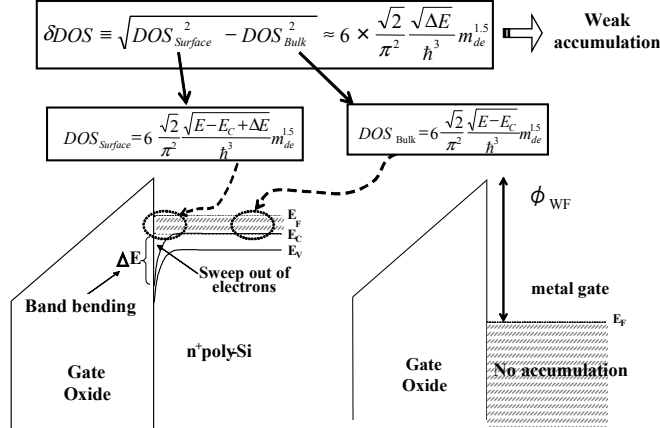Gate Oxide

metal gate

E_f

No accumulation

Fig. 4 Description of gate accumulation in polygate (Left): The right figure describes no existence of gate accumulation in metal gate at the same oxide field with the left. The square-root increase of DOS due to QRE (δDOS) causes the gate accumulation in polygate.

(a) Negative V$_G$ (b) Positive V$_G$

N$_{poly}$=1E20cm^{-3}
N$_{sub}$=6E16cm^{-3}
Gate accumulation
Hole subbands
OXIDE
P-Si
n$^+$poly-Si
6nm
V$_G$ = −3.1V

N$_{poly}$=1E20cm^{-3}
N$_{sub}$=6E16cm^{-3}
OXIDE
Electron subbands
Gate depletion
P-Si
n$^+$poly-Si
6nm
V$_G$=4V

Carrier Density (cm^{-3})
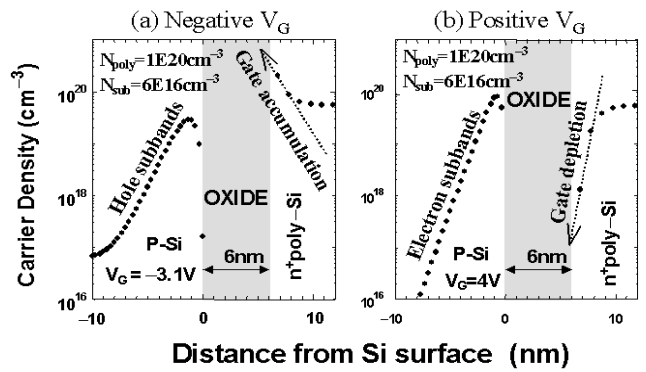Distance from Si surface (nm)

Fig. 5 Calculation result of carrier density profile in polygate while V$_G$ is negative (a) and positive (b): The gate accumulation is clearly shown at the poly-Si surface while the peak of holes subbands appears near the p-Si surface in (a). The gate depletion is clearly shown while the peak of electrons subbands appears near the p-Si surface in (b). The donor ion concentration in the bulk of the polygate is 6E19cm^{-3} due to incomplete ionization while the poly doping (N$_{poly}$) is set 1E20cm^{-3}.
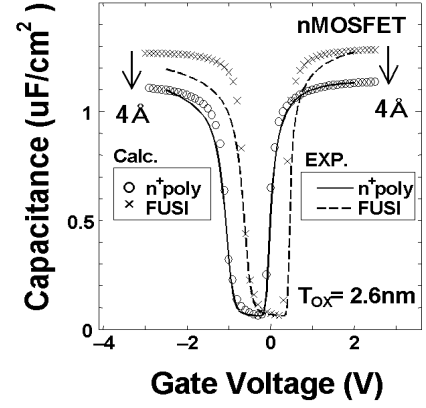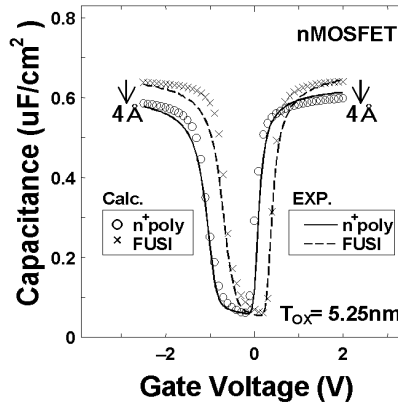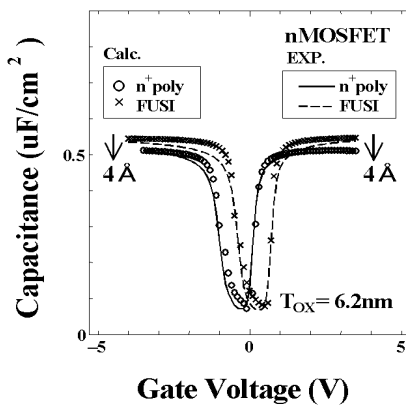

nMOSFET
Calc.
○ n$^+$poly
× FUSI
EXP.
— n$^+$poly
--- FUSI
4 Å
4 Å
T$_{OX}$= 6.2nm
Capacitance (uF/cm^2)
Gate Voltage (V)

nMOSFET
Calc.
○ n$^+$poly
× FUSI
EXP.
— n$^+$poly
--- FUSI
4 Å
4 Å
T$_{OX}$= 5.25nm
Capacitance (uF/cm^2)
Gate Voltage (V)

nMOSFET
Calc.
○ n$^+$poly
× FUSI
EXP.
— n$^+$poly
--- FUSI
4 Å
4 Å
T$_{OX}$= 2.6nm
Capacitance (uF/cm^2)
Gate Voltage (V)

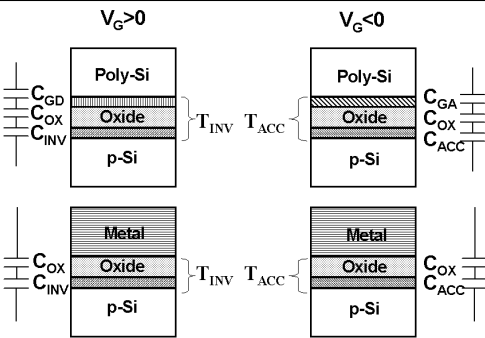Fig. 7 Measured and calculated CV characteristics of n$^+$ polygate and FUSI gate MOSFETs with p-Si substrate

V$_G$>0   V$_G$<0

Poly-Si
Oxide
p-Si
C$_{GD}$
C$_{OX}$
C$_{INV}$
T$_{INV}$ T$_{ACC}$
Poly-Si
Oxide
p-Si
C$_{GA}$
C$_{OX}$
C$_{ACC}$

Metal
Oxide
p-Si
C$_{OX}$
C$_{INV}$
T$_{INV}$ T$_{ACC}$
Metal
Oxide
p-Si
C$_{OX}$
C$_{ACC}$

Fig. 6 Equivalent circuits of metal gate and polygate

ΔT$_{OX}$ / T$_{OX}$ (%)
— ΔT$_{OX}$ = 4 Å
--- ΔT$_{OX}$ = 3 Å
○ N−ch. (EXP.)
× P−ch. (EXP.)
T$_{OX}$ (nm)
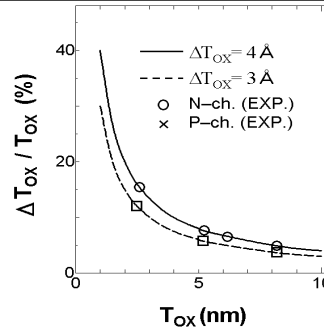
Fig. 8 Reduction of Tacc vs T$_{OX}$

Table 1 Extracted parameters from CV-fitting

N-Channel

T$_{OX}$ (nm)	N$_{SUB}$ (cm^{-3})	Φ_{WF} (eV)	ΔT$_{OX}$ (Å)
2.6	3E16	4.5	4
5.25	3E16	4.5	4
6.2	3E16	4.5	4
8.2	2E16	4.5	4

P-Channel

T$_{OX}$ (nm)	N$_{SUB}$ (cm^{-3})	Φ_{WF} (eV)	ΔT$_{OX}$ (Å)
2.5	3E16	4.4	3
5.2	3E16	4.4	3
8.2	3E16	4.4	3