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SPICE model of Pentacene Thin Film Transistor

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1. Introduction

In recent year, organic Thin Film Transistors have gained considerable interest due to their potential application in large area, low cost integrated circuit. Such applications include driving devices for active matrix flat panel displays, radio frequency identification tags, low-cost smart cards, etc. [1, 2] The efficient design of integrated circuit based on OTFT require SPICE model.[3]

In this paper developed a SPICE model of Pentacene Thin Film Transistor using HP a-TFT model of Hspice level 40. OTFT was made of Pentacene as semiconductor and cross-linked PVP as gate Insulator on glass substrate. The model was verified by the measured I-V characteristics of the fabricated Pentacene TFTs.

2. General Instructions

Fig.1 shows the structure of OTFT fabricated finally inverted staggered structure. PVP as organic gate insulator was spread through spin coating and baking after we patterned ITO on the glass. Then we evaporated the Pentacene using OMBD and deposited gold (Au) as top electrode.

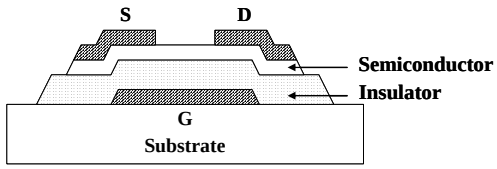

Fig. 1 OTFT Structure

Cross-linked PVP was mixed with PVP (poly-4-vinylphenol), PGMEA (propylene glycol monomethyl ether acetate) and poly (melamine-co-formalde hyde). Cross-linked PVP was spread through spin-coating by 30sec 3000rpm and baking 10min in 100℃ and 5min in 200℃. Pentacene was deposited in 80℃ of substrate temperature and 190℃ of source temperature. Then we evaporated gold as top electrode. In case of OTFT, mobility and threshold voltage are respectively 0.288cm^2/V·sec and -4V. Sub-threshold slope and on/ off ratio are 1.92 V/dec and 1.79×10^4.[4, 5]

We matched OTFT real data and simulation data using HP a-TFT model of Hspice level 40. Figure 2 shows the topology of the Level 40 model. First of all, we inputted parameters what was extracted from experience data. Mobility is 0.288cm^2/V-s. Threshold voltage is -4V. And dielectric constant and thickness of insulator are respectively 3.6 and 3000Å. Channel length and width are 100μ m and 2000μ m.

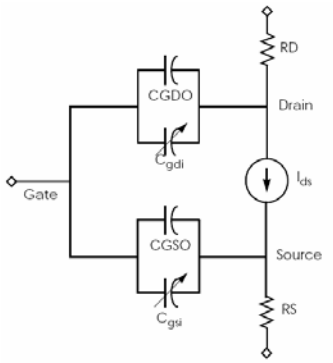

Fig 2. Level 40 Hp a-si TFT Topology

Table 1 is parameters of level 40 model. We simulated OTFT using these parameters.

Name	Comments	Values
UO	Mobility [cm^2/V-s]	0.288
Ueff	Effective Mobility [cm^2/V-s]	Calculated
ETA	Static feedback on threshold voltage [V^{-1}]	0
THETA	Mobility modulation [V^{-1}]	-0.007
GO	Conductance of TFT leakage current [ohm^{-1}]	1.0×10^{-11}
DEFF	Drain voltage effect for TFT leakage current	5
NFS	Fast surface state density [cm^2]	1.5×10^{19}
Cfm	Dielectric capacitance per unit area [F/cm^2]	1.06×10^{-8}
CGSO	TFT gate-to-source overlap capacitance [F]	87.3 p
CGDO	TFT gate-to-drain overlap capacitance [F]	87.3 p

Table 1. Hspice model parameters

In above threshold voltage region, we used THETA parameter of eq. (1). Sub-threshold current and leakage current were fitted using NFS, GO, DEFF of eq. (2) ~ eq. (7). Finally we inputted parameters of ac characteristic. CGDO and CGSO were calculated from eq (9), eq (10).

Hspice calculates other parameters.

$$ueff = f(uo, \eta, vgs, THETA) \qquad (1)$$

Eq. (2) is drain-source current in weak inversion region. Vt is thermal voltage.

$$Ids = idrain + f(GO, vgs, DEFF, vds) \qquad (2)$$

$$idrain = id \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right) \qquad (3)$$

$$von = f(vth, (vt \cdot xn)) \qquad (4)$$

$$xn = 1 + \left(\frac{(q \cdot NFS \cdot 10^4 \cdot W \cdot L}{Cfm}\right) \qquad (5)$$

$$Cfm = \frac{(\varepsilon 0 \cdot E1)}{T1} \qquad (6)$$

Eq. (7) is leakage current equation.

$$Ids = f(GO, vgs, DEFF, vds) \qquad (7)$$

Eq.(8) is capacitance equation of TFT. Fig. 3 is overlap capacitance of inverted staggered OTFT. And eq. (9)~(10) are overlap capacitance equation of OTFT

$$Cgd = Cgdi + CGDO$$
$$Cgs = Cgsi + CGSO \qquad (8)$$

$$CGDO = \frac{C_{PEN} \times C_{PVP}}{C_{PEN} + C_{PVP}} \qquad (9)$$

$$CGSO = \frac{C_{PEN} \times C_{PVP}}{C_{PEN} + C_{PVP}} \qquad (10)$$

Fig. 3

Finally we can confirm that simulation results was matched with experiment data except for increasing leakage current in cutoff region. Fig. 4 and Fig. 5 are transfer curve and output curve of simulation data and experiment data.

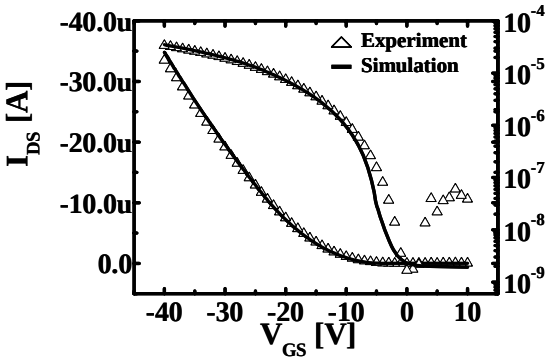

Fig. 4 OTFT Transfer Curve

We can see that simulation data is not equal to real data in sub-threshold region. The bigger sub-threshold current is, the more difficult match between simulation data and experiment data is. Because simulation equations in above threshold and sub-threshold region are different.

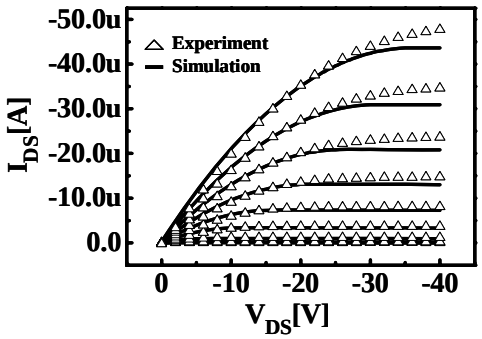

Fig. 5 OTFT Output Curve

Fig.5 shows that simulation data was saturated in $V_{DS} \geq V_{GS}-V_{TH}$ region but real data is increasing in same region.

3. Conclusions

We developed a SPICE model of Pentacene Thin Film Transistor using HP a-TFT model of Hspice level 40. The SPICE model of Pentacene TFT was made of parameters such as mobility modulation, fast surface state density, conductance of TFT leakage current and drain voltage effect for leakage current. The model was verified by the measured I-V characteristics of Pentacene TFT. We expect the spice model to be applied to AM-FPD, RFID, smart cards.

Acknowledgements

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