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# The annealing effects of GaN MIS capacitors with photo-CVD oxide layers

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## 1. Introduction

In the past years, GaN-based transistors such as, MES-FETs, HFETs, and HEMTs, have all been successfully developed [1]. However, the performances of these devices were not as good as expected. It is difficult to achieve high quality Schottky contacts. As a result, gate leakage currents are often large in the MESFETs, HFETs and HEMTs. Previously, the fabrications of GaN-based MIS-FETs and MIS-HFETs using $Si_3N_4$, $Ga_2O_3$, $Gd_2O_3$, $SiO_2$, MgO, $Sc_2O_3$, and stacked multi-layer oxide as the insulating material have all been demonstrated [2-4]. Previously, we reported that photo-assisted CVD (photo-CVD) can also be used to grow high quality $SiO_2$ on GaN and/or AlGaN epitaxial layers [5-7]. In this study, the effects of annealing on the properties of photo-CVD $SiO_2$/GaN MIS capacitors were investigated. The leakage current mechanisms of these capacitors will also be discussed.

## 2. Experiments

The GaN epitaxial films were grown on (0001) sapphire substrates by MOCVD. The structure consists of a 30nm-thick GaN nucleation layer deposited at 530°C and a 2.5 µm-thick Si-doped GaN layer grown at 1050°C. 50nm-thick $SiO_2$ layers were the deposited onto the GaN epitaxial layer by 150W $D_2$ lamp photo-CVD. During $SiO_2$ deposition, chamber pressure and substrate temperature were controlled at 0.9 torr and 300°C, respectively. In some cases, the as-grown samples were either annealed *in-situly* in the photo-CVD system or *ex-situly* in conventional furnace so as to improve the quality of the deposited photo-CVD $SiO_2$ layers. For *in-situ* annealing, the samples were annealed in either $O_2$ (i.e. sample A) or $N_2O$ (i.e. sample B) ambient under 150 Watt $D_2$ lamp irradiation for 2 hours. During *in-situ* annealing, chamber pressure and substrate temperature were controlled at 1.5 torr and 400°C, respectively. For *ex-situ* annealing, the samples were annealed in $N_2$ ambient for 2 hours at 800°C (i.e. sample C). Then, Al/$SiO_2$/GaN MIS capacitors were subsequently prepared by etching and metal evaporation. For comparison, capacitors with the as-grown samples without annealing were also prepared (i.e. sample D). Capacitance-voltage (C-V) and current-voltage (I-V) characteristics of the fabricated capacitors were then measured by an HP 4284B LCR meter and an HP 4156B semiconductor parameter analyzer, respectively.

## 3. Results and Discussion

As shown in Fig. 1, it can be seen clearly that leakage currents and breakdown fields observed from the three annealed samples (i.e. samples A, B, and C) were all much smaller and larger than that of the non-annealed sample (i.e. sample D), respectively. These results indicate that we can indeed improve the quality of photo-CVD layers significantly by performing post-deposition annealing. Among these samples, we achieved the smallest leakage current from sample C, which was *ex-situly* furnace annealed in $N_2$ ambient for 2 hours at 800°C. With an electric field of 4MV/cm, the leakage current measured from sample C was only $5.75\times10^{-8}$ A/cm$^2$. On the other hand, we achieved the largest breakdown voltage from sample A, which was *in-situly* photo-CVD annealed in $O_2$ ambient under 150 Watt $D_2$ lamp irradiation for 2 hours at 400°C. In other words, we achieved much better properties from samples A and C, as compared to samples B and D.

Frenkel-Poole emission and Field emission are two leakage current mechanisms that were commonly observed in MIS capacitors. Frenkel-Poole emission can be expressed by [8]

$$J \propto E \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_i\varepsilon_o})}{kT}\right] \qquad (1)$$

where $q$ is the electronic charge, $\phi_B$ is the barrier height, $\varepsilon_i$ is the insulator permittivity, $\varepsilon_o$ is the permittivity in vacuum, $k$ is the Boltzmann constant and $T$ is the absolute temperature. On the other hand, Field emission can be expressed by [8]

$$J \propto E^2 \exp\left[\frac{-8\pi\sqrt{2m^*}(q\phi_B)^{3/2}}{3qhE}\right] \qquad (2)$$

where $m^*$ is the effective mass, $\phi_B$ is the barrier height, and $h$ is the Planck constant. It can be seen clearly that the I-V characteristics of samples A and C could be fitted reasonably well by Frenkel-Poole emission model prior to breakdown. On the other hand, I-V characteristics of sample B could be fitted by Field emission model.

As shown in Fig. 2, for sample B, oxygen and nitrogen atoms diffused into the GaN epitaxial layer. Similar phenomenon was not observed from samples A and C. Since sample B was photo-CVD annealed in $N_2O$ ambient, it is possible that a gallium oxynitride layer was formed on the surface of this particular sample. We believe the different leakage current mechanism observed from sample B could be attributed to the formation of such a gallium oxynitride layer. Compared to samples A and C, the larger leakage current and the smaller breakdown filed observed from sample B should also be attributed to this gallium oxynitride layer.

Figure 3 shows room-temperature high frequency (i.e. 1 MHz) C-V characteristics of samples A, B and C. It was found that no hysteresis was observed as the gate voltage varied from +5 to –15V and then back to +5V for all these three capacitors. The lack of hysteresis indicates that the number of mobile ions in the insulator layer is negligibly small. From these C-V curves, we could determine the interface state density ($D_{it}$) using the standard high frequency capacitor method [9].

$$D_{it} = \frac{C_{ox}}{q}\left[\left(\frac{d\psi_s}{dV_g}\right)^{-1} - 1\right] - \frac{C_s}{q} \qquad (3)$$

where $C_{ox}$ is the oxide capacitance, $C_s$ is the depletion capacitance, $q$ is the electronic charge, $\psi_s$ is the band bending and $V_g$ is the gate voltage. Table I also lists measured $D_{it}$ of these capacitors. It was found that $D_{it}$ equals $1.96\times10^{11}$, $3.34\times10^{11}$, $1.63\times10^{11}$ and $8.4\times10^{11}$ $cm^{-2}eV^{-1}$ for samples A, B, C and D, respectively. In other words, sample D without any post-deposition annealing exhibited the largest $D_{it}$ among the four different kinds of capacitors. In contrast, interface densities of samples A and C were much smaller. These results agree very well with those observed from I-V measurements shown in Fig. 1.

It should be noted that although samples A and C both exhibit superior electrical properties, the annealing temperatures of these two capacitors were very different. Sample C was *ex-situly* furnace annealed in $N_2$ ambient at 800°C while sample A was *in-situ* annealed in the photo-CVD system in $O_2$ ambient under 150 Watt $D_2$ lamp irradiation at only 400°C. In other words, we could significantly reduce the annealing temperature and thus reduce thermal budget of the devices by using *in-situ* photo-CVD annealing. It is known that $D_2$ lamp emits a strong radiation between 110 and 170 nm, which can effectively decompose $O_2$. Therefore, $O_2$ molecules can be dissociated easily into oxygen atoms, such as O ($^3$p) and O ($^1$d), in our photo-CVD system. These excited oxygen atoms can thus effectively repair the dangling bonds which might exist in the oxide layer. We can thus achieve denser $SiO_2$ layers with enhanced electrical characteristics, even at low annealing temperatures. These results also suggest that photo-CVD annealing is an effective tool to improve the GaN MIS capacitors at low temperatures. Such an annealing method is also potentially useful for the fabrication of nitride-based MIS-FETs and MIS-HFETs.

## 4. Summary

In summary, GaN MIS capacitors with photo-CVD $SiO_2$ as the insulators were fabricated. The annealing effects of these capacitors were also investigated. It was found that we could significantly improve the electrical properties of the capacitors either by an *in-situ* annealing in $O_2$ at 400°C or by an *ex-situ* furnace annealing in $N_2$ at 800°C. The photo-CVD annealing is an effective tool to improve the GaN MIS capacitors at low temperatures.


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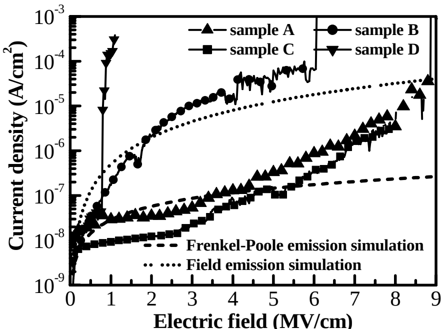


Fig. 1 Measured I-V characteristics of the four different kinds of Al/photo-CVD $SiO_2$/GaN MIS capacitors.

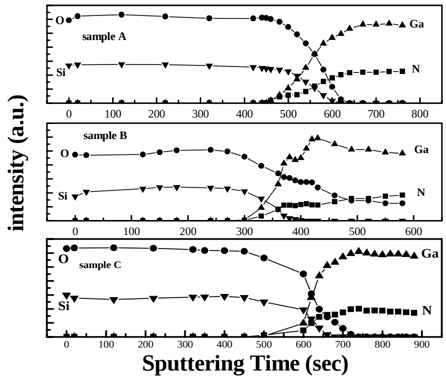


Fig. 2 AES depth profiles of samples A, B and C.

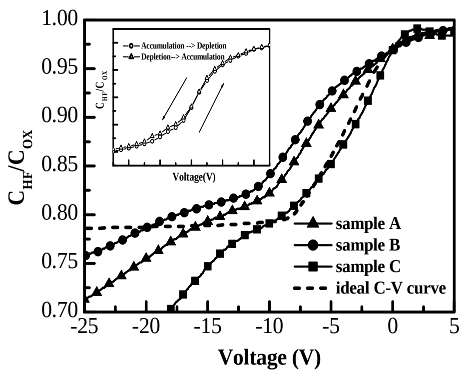


Fig. 3 Room-temperature high frequency (i.e. 1 MHz) C-V characteristics of samples A, B and C