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Nickel Germanide Formation on Condensed Ge Layer for Ge-on-Insulator Device Application

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1. Introduction

With the aggressive scaling-down of CMOS devices, both novel structures and materials with high carrier mobility are needed to continue improving the device performance [1,2]. Germanium device has recently re-attracted public attention as one of candidates to replace conventional silicon device because the germanium substrate has higher hole and electron mobility compare to that of silicon [3,4]. However, germanide formation technique is still at an early stage although the low parasitic resistance associated with the contact junction is essential to improve device performance. With this viewpoint, we studied about nickel germanide formation technique for applying to source and drain of Ge-on-Insulator (GOI) device with using the same way that is used in a multi-step RTA process. In this paper, we present the results of the physical structure, material properties and sheet resistance of nickel germanide formed on condensed Ge-on-insulator (GOI) substrates.

2. Experiments and Results

GOI layer formation

The fabrication process of GOI layer is schematically illustrated in Fig. 1. As illustrated in Fig. 1 (a)~(c), GOI layer was fabricated by the oxidation of a SiGe layer which was epitaxially grown on SOI wafer by ultra-high-vacuum chemical vapor deposition (UHV-CVD) varying the source gas ratio of Si_2H_6 to GeH_4. This method was inspired by the Ge condensation technique reported by Takagi, et.al. [5]. However, our technique is quite different from their technique because the gas ratio (Si_2H_6/GeH_4) is modulated with growth time in our technique. Using this method, GOI layer could be freely obtained and small surface roughness value (RMS=0.84nm) also could be realized on the GOI layer after removing oxide film as shown in Fig.1 (d).

Fig. 2 shows the XRD result of condensed GOI layer. As shown in the figure, it was confirmed that pure Ge(111) could be obtained by the condensation technique. Figure 3 shows the Raman spectroscopy measurement results before and after the Ge condensation processes. In the figure, we confirmed that GOI layer was successfully formed because the peaks of Si-Ge and Si-Si in the SiGe layer observed in the spectrum before condensation process disappeared completely in the spectrum after condensation process.

Nickel germanide formation

Nickel germanide formation was studied with GOI layer formed by the Ge condensation method as described above. An multi-step annealing with single temperature rising period (50°C/sec) and holding period (30sec each) has been applied to the nickel film with the thickness of 10nm, 20nm and 30nm deposited on the condensed GOI layers as shown in Fig.4 (a). With this annealing method, very low sheet resistance could be obtained at 500°C in the case of 20nm thick nickel film as shown in Fig. 4 (b). Figure 5 shows the transmission electron microscope (TEM) image of the nickel germanide which was obtained by annealing the nickel film with the initial thickness of 20nm. As shown in the figure, the nickel germanide with the thickness of 30 nm has been successfully formed. And it is observed that a relatively uniform thickness and a smooth surface are achieved in the Ni germanide formed using our method, which explains the sufficiently low sheet resistance previously shown in Fig. 4 (b). Figure 6 shows the XRD results obtained in the sample with the same condition as that of TEM sample. The diffraction lines of NiGe(111), NiGe(121) and NiGe (002) are observed. Figure 7 shows the SIMS profiles of fabricated nickel germanide. We can clearly see in the figure that the NiGe layer with the thickness of ~20nm is obtained on the buried oxide as a result of the nickel germanidation.

3. Conclusions

We proposed a new method to form a nickel germanide layer on the GOI wafer formed by Ge condensation technique using multi-step annealing method. NiGe layer with low sheet resistance was obtained at 500^{o}C. We confirmed that this method is suitable for nickel germanide formation technique to fabricate GOI MOSFETs with low source/drain resistances.

References

[1] Rritze M et al 2004 IEEE Electron Device Lett. 25 p.220
[2] Keiji Ikeda, Yoshimi Yamashita, Akira Endoh et al 2002 IEEE Electron Device Lett. 23 p.670
[3] Shang H. L. et. al., 2002 IEDM tech. Dig. p.441
[4] Huang C. H. et. al., 2003 VLSI tech. p.119
[5] Shu Nakaharai, Tsutomu Tezuka, Naoharu Sugiyama, Yoshihiko Mriyama, and Shin-ichi Takagi, Appl. Phys. Letter, Vol.83, No.17, pp.3516-3518, 2003.

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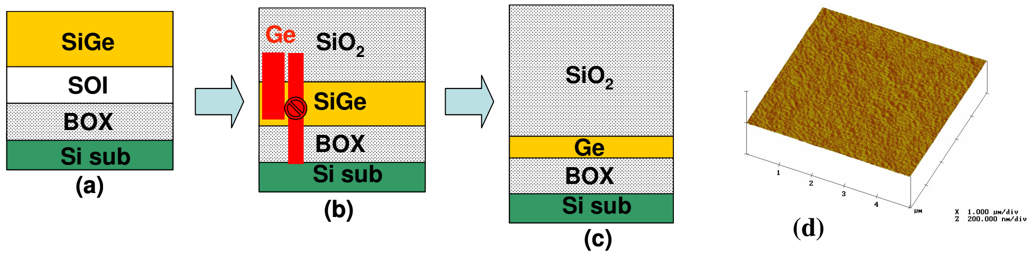

Fig.1. Process sequence for germanium condensation (a) ~ (c) and AFM image of GOI layer formed by germanium condensation (RMS=0.84nm) (d).

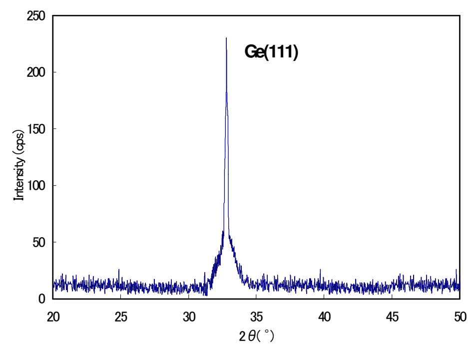

Fig.2 XRD pattern of GOI layer formed by Ge condensation.

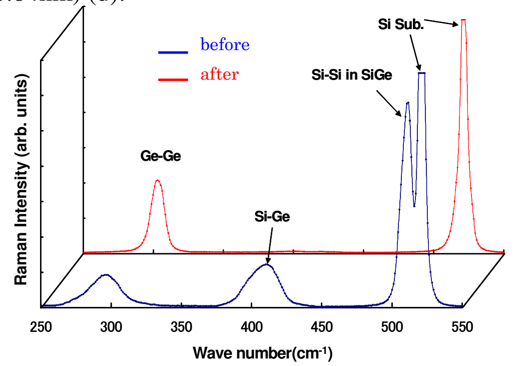

Fig.3 Raman spectra of GOI layer formed by Ge condensation.

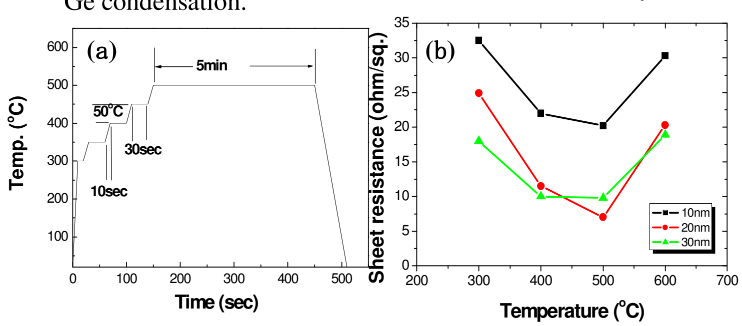

Fig. 4 Temperature history(a) and sheet resistance of nickel germanide as a function of annealing temperature(b).

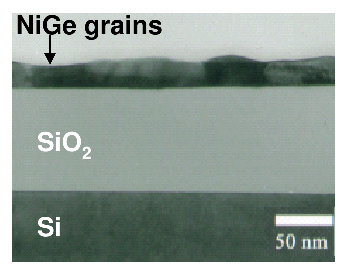

Fig. 5 TEM image of NiGe film with an initial nickel thickness of 20 nm.

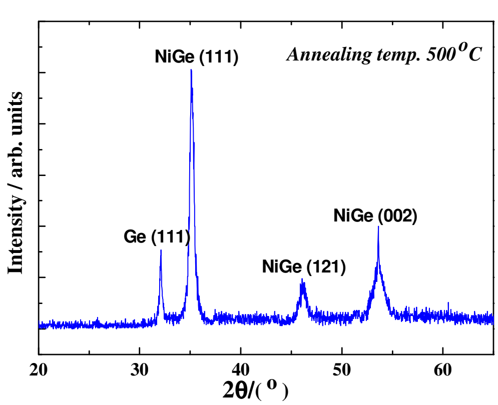

Fig. 6 XRD pattern of nickel germanide.

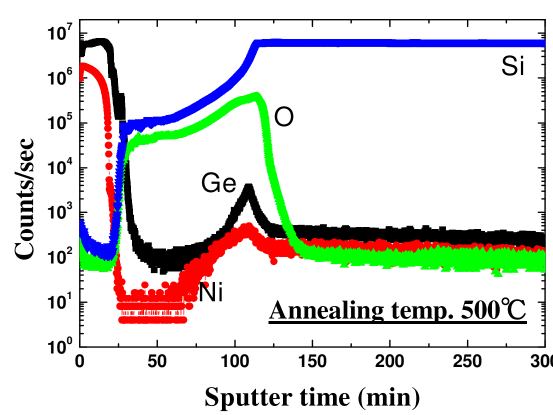

Fig. 7 SIMS profiles of NiGe/SiO2/Si substrate structure formed by nickel germanidation of GOI.