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Deep Trench Etching for Chip-to-Chip Three-Dimensional Integration

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1. Introduction

In recent years, three-dimensional (3D) integration technology has attracted much attention since the technology offers the possibility that interconnection problems would be solved. 3D LSI has great advantages such as parallel processing, low power consumption, short wire length and high-speed operation. We have previously described the fabrication of 3D LSI by wafer-to-wafer stacking method [1,2]. However, the wafer-to-wafer stacking method gives rise to the reduced overall yield since the total yield of stacked wafers is given by multiplying the yields of the respective wafers. In addition, we can not stack the wafers with different chip size in the wafer-to-wafer stacking method.

To solve these problems in the wafer-to-wafer stacking method, we have developed a new chip-to-chip 3D integration technology, in which the deep trenches for buried interconnections are formed after an LSI wafer is diced into many chips. In this paper, we describe an advanced deep trench etching for chip-to-chip 3D LSI integration technology.

2. Chip-to-chip 3D integration technology

Figure 1 shows the cross-sectional structure of 3D LSI fabricated by the chip-to-chip 3D integration technology. Completed LSI chips are vertically stacked in the chip-to-chip 3D integration technology. Therefore, the deep trenches for buried interconnections are formed in the completed LSI chips. It is more difficult to form the buried interconnections in a completed LSI chip fabrication sequence for chip-to-chip 3D integration technology is shown in Fig.2. As is shown in the figure, first of all, an LSI wafer is diced into many LSI chips after all of chips in the LSI wafer were tested. Then, known good dies (KGDs) are selected and these KGDs are temporally glued to a supporting material using a photoresist as adhesive. We can use a Si wafer, a quartz glass and so on as a supporting material. After gluing the KGDs to supporting material, the buried interconnections and the metal microbumps are formed. Then, the KGDs are temporally glued again to another supporting material and the first supporting material id removed. After that, the KGDs are thinned from the backside to expose the bottom of buried interconnection and the metal microbumps are formed at the bottom of the buried interconnections. These thinned KGDs with buried interconnection and the metal microbumps are glued to another KGDs with a supporting material and then the second supporting material is removed. By repeating this sequence, we can fabricate 3D LSIs with many stacked layers. Figure 3 shows an SEM cross-sectional view of buried interconnections formed in a Si wafer. As is clear in the figure, the buried interconnections completely filled with conductive material of poly-Si are successfully formed in the case of using Si wafer. We used the inductively coupled plasma – reactive ion etching (ICP-RIE) and Bosch's process to form the deep trenches for the buried interconnections. An etching step using SF_6 gas and a passivating step using C_4F_8 gas are alternately employed in the Bosch's process to form the deep trenches. The wafer was cooled down from the backside in plasma etching in order to prevent the wafer temperature rise due to the plasma reaction since the wafer temperature rise during plasma etching causes poor etching profiles. However, we have to use the adhesive with very poor thermal conductivity to glue the KGDs to the supporting material in our chip-to-chip 3D integration technology. As a result, this adhesive layer prevents the chips from cooling and caused poor trench profiles as shown in Fig.4 where the etching profiles of deep trench with the depth of 42um obtained in a Si wafer and a bare Si chip are compared. As id obvious in the figure, the trench profile with a slight taper along the trench depth is obtained in trench etching using a wafer. The trench width was 3.2um and 1.9um at the top and at the bottom, respectively. Such trench with a forward taper is desirable for the buried interconnection since it is suitable for the complete filling of trench by a conductive material. On the other hand, the trench profile with a reverse taper was obtained in trench etching using a bare chip as shown in Fig.4 (b) when the identical etching condition is employed. The trench width was 3.0um and 3.2um at the top and at the bottom, respectively. Then, in order to obtain the desirable trench profile in a bare chip, we evaluated the effects of etching time (etching duration) and passivation time (passivation duration) on the trench etching profiles using bare Si chips and consequently found that the ratio of etching time to passivation time has the dignificant effect on the trench etching profiles as shown in Fig.5 where the trench widths at the top and at the bottom are plotted as a function of the ratio of etching time to passivation time. It is clear from the figure that the bottom width of trench dramatically increases as the ratio of etching time to passivation time increases whereas the top width is hardly affected by the ratio of etching time to passivation time. We have succeeded in obtaining the desirable trench profile with forward taper by optimizing the ratio of etching time to passivation time as shown in Fig.6. The trench width was 3.0um and 2.4um at the top and at the bottom, respectively.

3. Deep trench etching through interlayer dielectric

LSI chips have thick interlayer dielectric films on a Si substrate. Therefore, in order to form the buried interconnections in the completed LSI chip, we have to form them through these interlayer dielectric films to the Si substrate. However, in the trench etching using the samples with the thick silicon oxide on the Si substrate, a serious undercut of Si underneath the silicon oxide due to the enhanced side etching of Si is often produced because the trajectory of ionized etching species is distorted by the charging-up of the silicon oxide during plasma etching as described in Fig.7 (a). Such undercut results in the incomplete filing of conductive material into the trench. To solve this problem, we proposed to deposit a protection film on the side surface of trench formed into the interlayer dielectric of silicon oxide as shown in Fig.7 (b). The Si trench width underneath the silicon oxide is reduced by the amount corresponding to the thickness of protection sidewall film. As a result, we can form the deep trench without the serious undercut underneath the silicon oxide after removing the protection sidewall film. Figure 8 shows an SEM cross-view of the trench with protection sidewall film formed into the interlayer dielectric of silicon

oxide. The protection sidewall film was formed using C_4F_8 gas. It is clear in the figure that the protection sidewall is successfully formed only on the side surface of trench formed into the silicon oxide. The relationship between the deposition time of protection sidewall film and the amount of side etching (undercut) is shown in Fig.9. As is clear in the figure, the amount of side etching is significantly reduced as the deposition time and hence the protection sidewall film increase. Figure 10 shows an SEM cross-sectional view of the trench formed through the interlayer dielectric of silicon oxide into the Si substrate by using the method as describe above. The amount of side etching was reduced to around 55nm which does not prevent the trench from being completely filled with a conductive material. Thus, the desirable trench etching profile without the undercut was obtained in a bare Si chip glued to a supporting material by optimizing the deposition time of protection sidewall film and the ratio of etching time to passivation time.

4. Summery

We proposed a new chip-to-chip 3D integration technology in which the completed LSI chips are vertically stacked and electrically connected by the buried interconnections. In order to fabricate the buried interconnections in the completed LSI chip, we successfully formed the trench with the desirable etching profile without the undercut through the interlayer dielectric of silicon oxide into the Si substrate using bare Si chips by optimizing the deposition time of protection sidewall film and the ratio of etching time to passivation time.

Acknowledgements:

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References:

[1] H. Kurino, *et al.,* IEDM Technical Digest, 879, (1999)
[2] K. W. Lee, *et al.,* IEDM Technical Digest, 165, (2000)

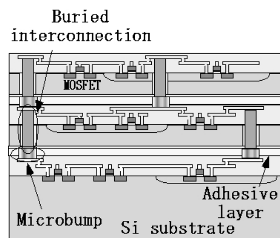


Fig1. Cross-sectional structure of 3D LSI.

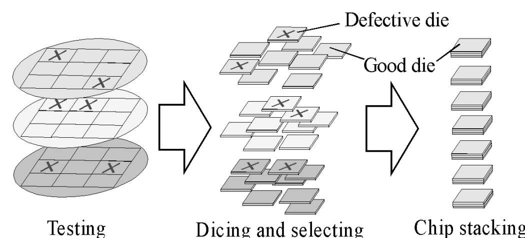


Fig.2 Fabrication sequence for the chip-to-chip 3D integration technology.

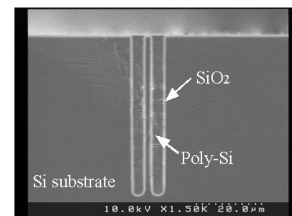
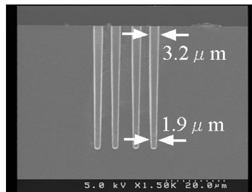
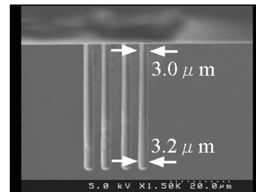


Fig.3 SEM cross-sectional view of poly-Si buried interconnection.



(a) In Si wafer



(b) In bare Si chip

Fig.4 SEM cross-sectional view of trench profile.

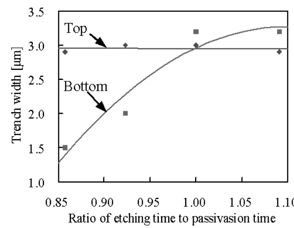


Fig.5 Trench width at the top and at the bottom as a function of etching time to passivation time.

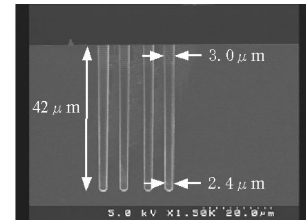
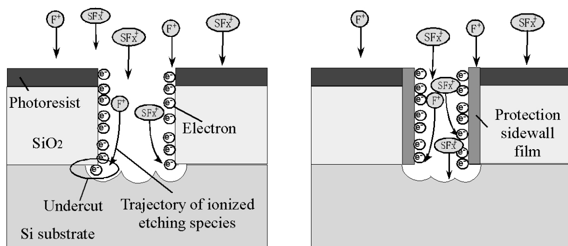


Fig.6 SEM cross-sectional view of deep trench with forward taper formed bare Si chip glued to supporting material.



(a) Without protection film (b) With protection film

Fig.7 Side etching of Si underneath silicon oxide in forming trench through silicon oxide into Si substrate.

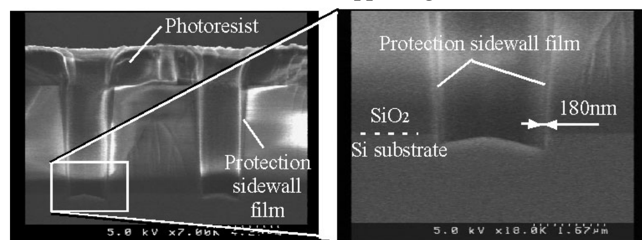


Fig.8 SEM cross-sectional view of trench with protection sidewall film formed into silicon oxide.

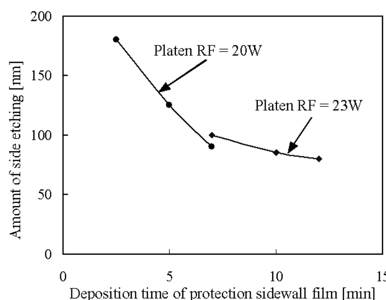


Fig.9 Relationship between the deposition time of protection sidewall film and the amount of side etching.

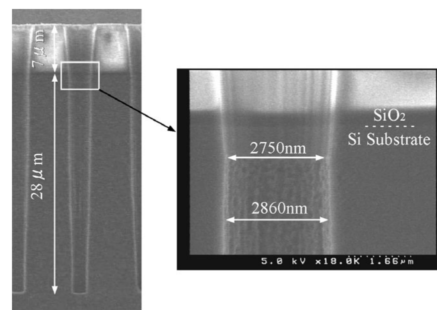


Fig.10 SEM cross-sectional view of trench formed through silicon oxide into Si substrate in bare Si chip.