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High Aspect-Ratio Through-Wafer Interconnections with Thick Oxidized Porous Silicon Sidewall Via

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1. Introduction

The through-wafer interconnections have a lot of merits for the application of high performance, low cost, and high density integration of RF systems and devices, and for the three dimensional (3-D) IC packages due to their small sizes and small parasitics.

The HRS wafer[1] is generally used as the substrate for the via. But with those materials it is hard to integrate the active circuits on the wafer. With the CMOS grade silicon wafers, thin insulating films such as 500 nm SiNx was used as a via liner[2]. But this liner is thin and changing dramatically with its depth due to CVD process limitation.

In this paper, we propose the smart silicon through-wafer vias with the thick oxide sidewall and show its fabrication process and evaluation results.

The use of the thick OPS makes it easy to use ordinary CMOS grade silicon wafers as the RF substrate and its 3-D packages without the use of HRS wafers. And it is possible to fabricate both the integrated circuits and the RF circuits on the same wafer. All these schematics imply that the small and high density stacking of chips is possible with this design.

2. Fabrication

Fig.1 shows the schematics of the proposed via and an example of its application to the RF module. These vias have the oxidized porous silicon(OPS) side walls, the plated copper fillings, and the bump pads on the Benzocyclobutene(BCB) layer.

On (100) boron-doped 5 ohm*cm silicon wafer, the via holes were made with the inductively coupled plasma (ICP) deep reactive ion etching (RIE). The etched depth was 250 μm with 70 μm diameter, and the anisotropy of the via was 87°. To get the strain free thick oxide sidewall, the wafer and the inside of the via holes were anodized and oxidized[3,4]. The thickness of the OPS layer was about 26 μm, and that of the OPS side wall of the holes was about 18 μm. Fig.2 (a) shows the cross-section of a via with thick OPS sidewall. The wafer was then back lapped and polished to the final thickness of 240 μm to get the through-holes. The via holes are filled with the copper by electroplating. The shape of the copper barrel is shown in Fig.2 (b).

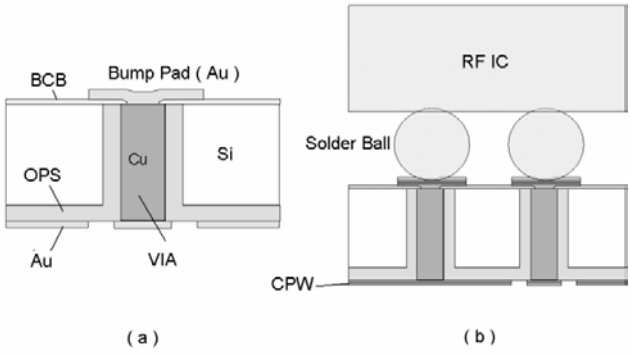

Fig. 1 Schematic Diagram of the proposed through-wafer via.
(a) proposed schematics (b) a concept of RF module on the vias.

And then the photo-BCB, Cyclotene 4024-40 of Dow Chemical, of 4 μm was coated and cured . The size of contact opening was 60 μm diameter.

Both side of the wafer is processed with the Au-plating to get the flip chip bonding pad and RF/MW circuits[3].

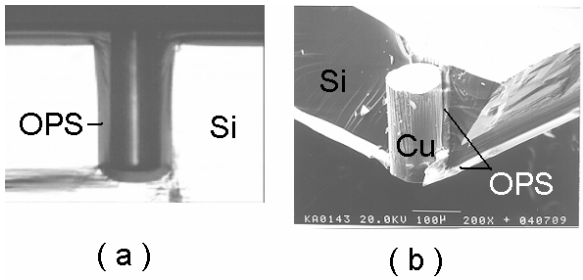

Fig. 2 (a) cross-sectional view of the via with OPS side wall
(b) SEM photograph of the plated copper barrel filled in the via

To characterize the parameter of the via, a via shorted to the ground was fabricatedFig.3 (a) shows the metallic inter-connection structure. Fig.3 (b) shows the BCB-side metal patterns. The thickness of Au plated on BCB side is 15 um and the one of whole OPS side is 3 um. The diameters of all vias are 70 μm each, and that of the PAD is 200 μm to meet the size of the solder bump for the flip-chip bonding. The size of MLIN is 74 μm wide and 206 μm long.

3. Test and Results:

On wafer one port S-parameter measurements were done on the via, shorted to the ground, by using HP8720C network analyzer and Cascade microwave GSG

probes. Measured reflection coefficient, S11, data are plotted in the Smith chart in Fig.4 (b).
Fig.4 (a) shows the equivalent circuit of this shorted via. In the case of VIA Grounded, two vias are connected directly to the ground pads with their parallel barrels. So each parameter was set in proportion to its geometric shape.

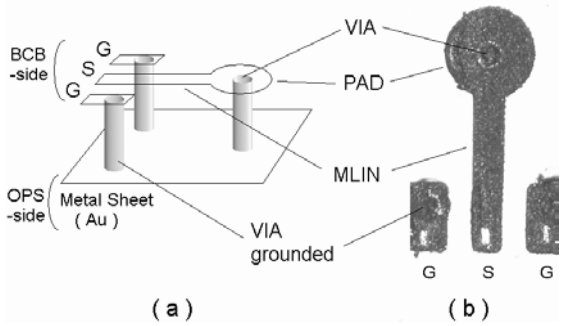

Fig. 3 (a) the metallic structure of the via shorts
(b) top-view of the metal pattern of the BCB-side

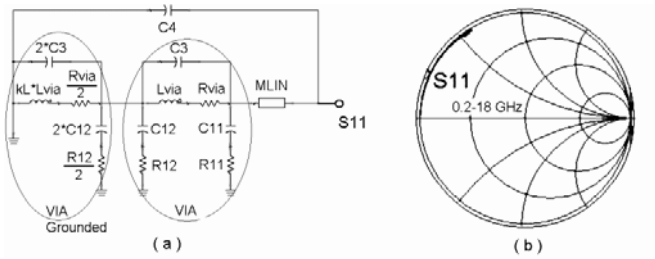

Fig. 4 (a) the modelling circuit diagram of the via shorts
(b) S11 data measured

For the extraction of the via model circuit, the measured S11 data were smoothed and the parameters of the model circuits of Fig.3 (b) were optimized to minimize the magnitude and phase errors for the S11 values. Table I shows the optimized parameter set for the through-wafer via model. The optimized Lvia is of 0.079 nH and Rvia is 0.056 Ohm.

Fig.5 shows the real and imaginary parts of S11 of the measured and the calculated. It shows the S11 parameters fit well (<1%). They are in good agreements.
By using the straight round wire approximation[5], 0.09 nH and 0.02 Ohm at 2 GHz were calculated. They are relatively in good agreement with this work.

In the case of HRS wafer[1], the parameters of a via which is 70 μm diameter and 400 μm long is 0.4nH and 0.15 Ohm. This work shows less inductance per length compared to the one on HRS wafer.

4. Conclusion

The through-wafer via with the thick oxide sidewall on the CMOS grade silicon wafer was fabricated and its RF model was extracted by using the RF parameter optimization of the via shorts. The inductance is 0.079 nH and the series resistance is 0.056 Ohm for the copper via of

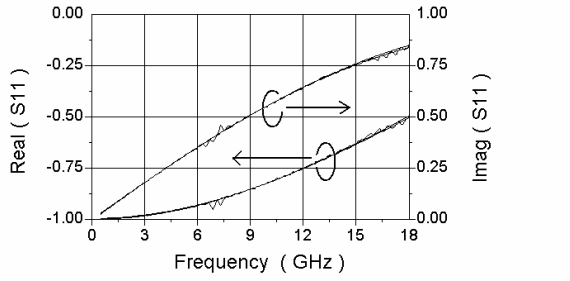

Fig. 6 S11 for the real and the imaginary components

Symbol	Quantity	Symbol	Quantity
Rvia	0.056 Ohm	Lvia	0.079 nH
C11	62.1 fF	C12	50.4 fF
R11	1 K Ohm	R12	1.32 M Ohm
C3	1.1 fF	C4	2.3 fF
kL	0.57		

Table. I The optimized parameter set

240 μm long and 70 μm diameter. The resistivity of the silicon wafer is 5 Ohm*cm and the thickness of the OPS side wall is about 18 μm. The other paracitics are less than 60 fF.

This through-wafer via with OPS sidewall is applicable to the compact and high density integration or flip-chip bonding of RF module or 3-D packages.

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