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P3-1

3D Device Simulation for Neutron-induced Latch-up in CMOS Devices

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1. Introduction

Along with recent scaling of CMOS devices down to sub-100nm, neutron induced single event effects (SEEs) would be serious concern in reliability. Among SEEs, neutron induced microlatch, which is the phenomenon the drain current increase spreads over multiple cells during beam irradiation, is emerging as a new serious error mode, though their clear-cut physical mechanism is not identified [1,2,3].

We elucidated microlatch physics for the first time using a 3D device simulator to analyze parasitic bipolar actions in 130nm multiple CMOS bulk devices caused by secondary ions produced by a single neutron incidence.

2. Method

We select Mg ion as a candidate secondary ion produced from non-elastic scattering Si(n,α)Mg under environmental neutron field. The energy of Mg ion is fixed at 0.3, 0.5, 0.65, 0.8, 1, 3, 10MeV to cover the average energy range calculated with our soft-error simulator CORIMS [4]. Corresponding LETs of Mg ions in Si substrate are 17, 26, 32, 38, 45, 92, 123fC/μm respectively.

We use Davinci^{TM} to analyze transient responses after the ion bombardment, applying SRH and Auger recombination models, Lombardi's surface mobility model, and impact ionization model.

Firstly, we perform simulation for single NMOS with 130nm gate length formed on deep-n-well. Then, we make similar simulations for single CMOS region including one PMOS-NMOS pare, and lastly for the region including four PMOS-NMOS pares.

Only results for 10MeV Mg ion are shown below due to the space limitation.

3. Result

Single NMOS region

Figure1 shows the configuration of single NMOS with two ion tracks. Track A is perpendicular from the top to bottom through the NMOS1 node. Track B is parallel with the source-drain direction in the well. In other word, track A passes through the p/n junction between the p-well and deep-n-well, and track B does not pass through the referred p/n junction.

Figure2 shows node current transient for 10MeV Mg ion passing track A and B, respectively. For track A, two peaks appear in the current transient at around 10ps and 1ns. In contrast, for track B, only 10ps peak appears. From this result, it is considered that the 1ns peak is caused by parasitic bipolar action in the p/n junction between the n+ node and the deep n-well, though the 10ps peak is caused by parasitic bipolar action in the p/n junction between the source and drain. Total charges collected to the node are about 4 times larger than the charge deposition along the tracks. This charge "amplification" would be caused by parasitic bipolar action as displayed in Fig.1. This insight agrees well with the theory of "snapback" by Beitman [5].

Single CMOS region

In single CMOS region, we perform simulation for the ion track from PMOS side toward NMOS side in the well. Figure3 shows node current transient for 10MeV Mg ion.

Both 10ps and 1ns peaks appear in the current transient as seen in Fig.3. It is considered that 1ns peak is caused by parasitic bipolar action in the p/n junction between the n+ node and the n-well. Actually n-well and deep-n-well are electrically identical, this bipolar action is similar to that in the p/n junction between the n+ node and the deep-n-well for single NMOS. But unlike Fig.2, the current saturates after 1ns peak at the order of 1mA, which is much larger than normal source-drain current.

Considering these results, we would conclude that the abnormal current saturation level in the CMOS structure is triggered by snapback due to parasitic bipolar transistor in p/n junction between the n-well and the p-well, as displayed in Fig.4. Subsequently, it may result in latch-up due to parasitic thyrister composed of an NPN transistor formed from p-well as base, n-well as collector and n+ node as emitter, and a PNP transistor formed from n-well as base, p-well as collector and p+ node as emitter. Then, the current path is formed between n-well and p-well as commonly seen in latchup event [6].

Whole four CMOSs region

In four CMOSs region, we perform simulation for the ion track from one PMOS side toward counterpart NMOS side in the well, as shown in Fig.5, similarly to single CMOS region.

Figure6 shows node current for Mg ion of 10MeV. Initial LET is equivalent to the charge deposition density of 123fC/μm in Si. Node1 is the node of the CMOS which the ion track enters, and node2 to 4 are those of adjacent CMOSs.

Currents of all nodes show the same tendency. Thus, all four CMOSs, not only one CMOS in which the ion penetrates, fail by one local ion shot. This result is highly consistent with the feature of microlatch. At higher ion energy, more than four nodes may naturally fail by one local ion shot under this mechanism.

By simulating at other ion energies, the threshold ion energy that node currents saturate is estimated at about 650keV, where the charge deposition density is 32fC/μm.

Figure7 shows the current transient as ion energy of Mg is 500keV, that is, the LET is 26fC/μm. Blank of lines from 0.1ns to 1ns means zero or negative values. In this condition, the current is not saturated.

As shown in Fig.8, the n-well voltage reaches about 0.2V in the minimum on the condition in Fig.6. While, as shown in Fig.9, this voltage reaches 0.25V on the condition in Fig.7. It is considered that as the ohmic drop of well voltage exceeds 1.0V, the parasitic bipolar between n-well and p-well turns on, and the node current saturates.

4. Conclusions

The behavior of CMOS due to neutron irradiation is analyzed by using 3D device simulation with single NMOS, single CMOS, and four CMOSs models. For the single NMOS model, the collected charge to the drain node is more than the deposited charge by Mg ion, as the ion passes through the p/n junction in the well, not necessarily at storage node. It is also found with one to four CMOS cell model that current continues to flow from n-well to p-well with a saturation order of 1mA in all four cells by Mg ion hit in local cell. According to these result, it is interpreted that microlatch is multi-cell non-destructive latch-up triggered by snapback.

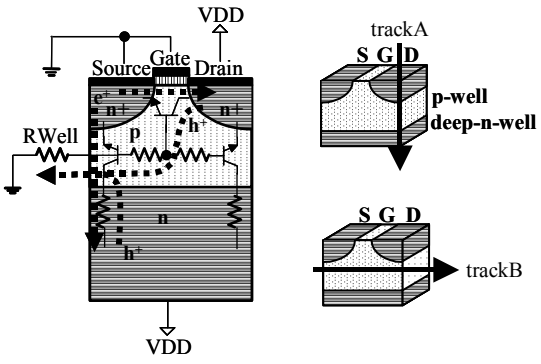

Figure1 Single NMOS configuration and schema of snapback

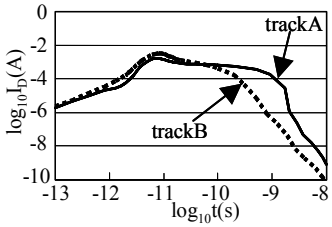

Figure2 Current transient for single CMOS

References

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[6] R. Troutman: 'Latchup in CMOS Technology - The Problem and It's cure': 1st ed., Kluwer Academic Publishers (1986)

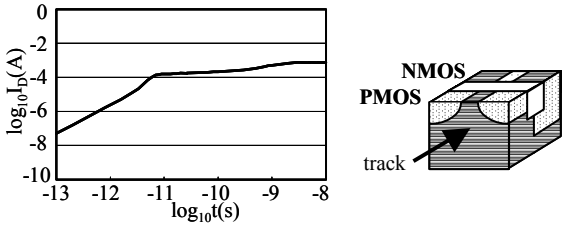

Figure3 Current transient for single NMOS

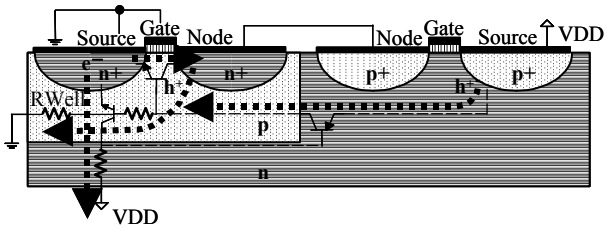

Figure4 Schema of latch-up

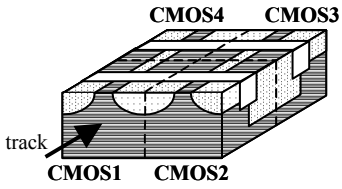

Figure5 Four CMOSs configuration

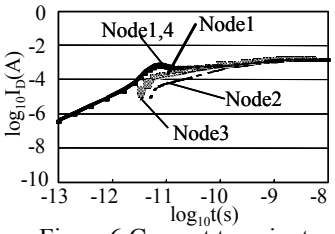

Figure6 Current transient (ion energy: 10MeV)

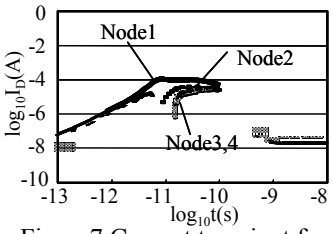

Figure7 Current transient for (ion energy: 500keV)

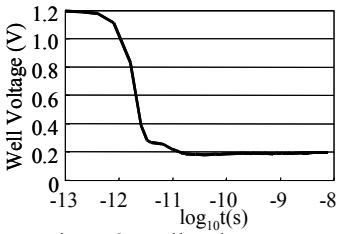

Figure8 Well voltage transient (ion energy: 10MeV)

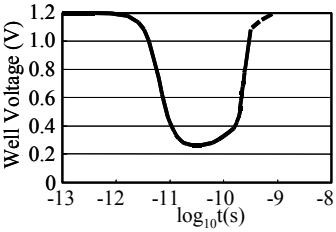

Figure9 Well voltage transient (ion energy: 500keV)