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Impact of Oxide Thickness Fluctuation on MOSFETs Gate Tunnelling

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1. Introduction

Standby power dissipation becomes one of the biggest challenging issues in today's ULSI system design [1]. At 90nm technology node, it can approach the level of dynamic power dissipation for some long standby application if low power design methods (such as dual threshold voltage technology) fail to be introduced. Standby power dissipation is mainly caused by subthreshold and gate leakage currents. As a result of aggressive scaling, gate leakage current can surpass subthreshold current at around 65nm technology node if suitable high-k materials fail to be introduced. Bearing in mind that the magnitude of intrinsic parameter fluctuation steadily increases with the device scaling [2], and the gate tunnelling current increases exponentially with the reduction of the oxide layer thickness, the oxide thickness fluctuation may have a big impact on gate tunnelling behaviour

2. Simulation Method

In this work, we study the random variation in the gate tunnelling current introduced by the oxide thickness fluctuations in a 30nm physical gate length MOSFETs with a mean value of the oxide thickness 1.2nm.

Although to understand properly the problems associated with gate leakage variations 3D simulations are needed, in this paper we use 2D simulation with MEDICI to illustrate the importance of this effect. Gundlach tunnelling model is used and direct gate tunnelling in long channel MOSFETs at various bias conditions are calibrated against the experiment data [3]. Fig.1 shows the calibration result, which yields an effective electron mass of $0.535m_0$ in oxide. The 30nm device structures are shown in Fig.2, where one overlap and one underlap case have been chosen in order to clearly show edge direct tunnelling effects. Correlation length λ=1.8nm and RMS Δ=0.3nm are used to generate random oxide thickness fluctuation pattern following the methodology described in [4]. Two gate leakage conditions have been considered: "condition A" with V_{ds} fixed to zero, and V_g sweeping from subthreshold to strong inversion region, "condition B" with V_g fixed to zero, and V_{ds} sweeping from 0 to Vdd. The extreme cases of these two conditions represent two typical gate leakage modes in circuit, like the simple inverter illustrated in Fig.3.

3. Results and Discussions

Fig.4 (a) shows the distribution of direct tunnelling current between the gate and the substrate for $V_g > 0V$ over an ensemble of 200 devices for overlap structure, and the counterpart underlap structure has similar result (Fig.4 (b)). For leakage current at V_g = 1V, the mean value of gate tunnelling are all around 450nA/μm, which shows that in "condition A" the gate to channel tunnelling dominates, and edge direct tunnelling has no significant effects on leakage current. Inset graphs in Fig. 4 show the distribution of gate tunnelling current at V_g =1V, they roughly follow normal distribution, and the standard deviations are approximately 40% of mean value, which is quite significant and should be taken into account in circuit design. Fig.5 shows the direct tunnelling current under "condition B". As for the overlap structure, the mean value of gate tunnelling current at $V_{ds} = 1V$ is 30nA/μm, which is almost twenty times larger than underlap case. This indicates edge direct tunnelling plays an important role for "condition B". Inset graphs in Fig.5 show the distribution of gate tunnelling current at $V_{ds} = 1V$, which do not follow a normal distribution. If the standard deviation is used as a measure of the magnitude of fluctuation, its value is 80% of the mean gate leakage current for the overlap structure and 88% for the underlap structure. Although underlap structure has much better gate tunnelling performance at "condition B", for circuits in which "condition A" is present with considerable probability, little benefits is gained by change device structure from overlap to underlap from gate leakage power dissipation point of view.

4. Conclusion

For 30nm physical gate length device with 1.2nm physical oxide thickness and 1V supply voltage, the worst-case gate leakage current will well above 100nA/μm ("condition A"), and become the dominated part in device leakage current. Furthermore, oxide thickness fluctuation will cause big variation in gate tunnelling current. Further study need to be done to fully assess their impacts on circuit standby power and functionality.

References

[1] H. S. Momose et al., "Prospects of low-power, high-speed MPU's using 1.5nm direct-tunnelling gate oxide Si MOSFETs", Solid-State Electron. **41** (1997) 707.

[2] A. Asenov, "3D statistical simulation of intrinsic fluctuations in decanano MOSFETs induced by discrete dopants, oxide thickness fluctuations and LER", Proc. SISPAD2001, (2001) 162.

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[4] A. Asenov, S.Kaya and J. H. Davies, "Intrinsic threshold voltage fluctuations in Decanano MOSFET's due to local oxide thickness variations ", IEEE Transactions on Electron Devices, **49** (2002) 112.

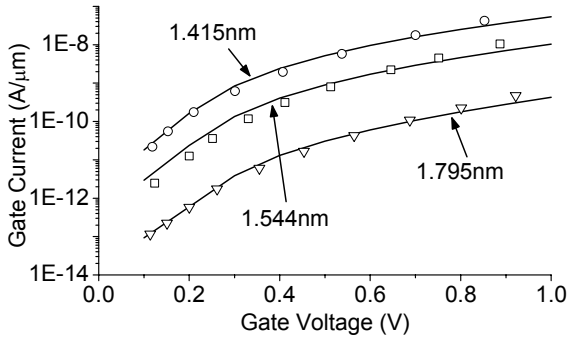
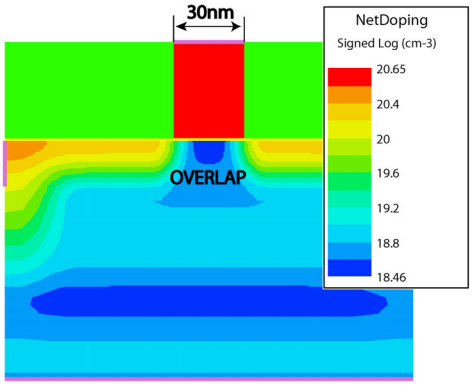
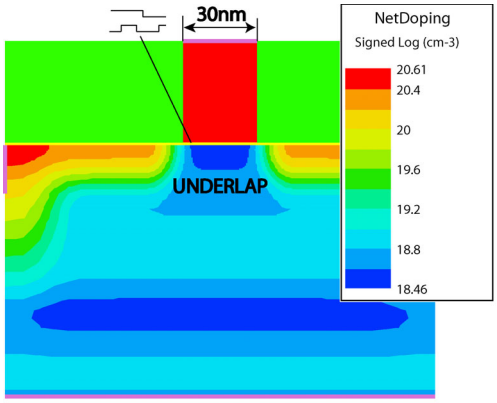


Fig.1 Calibration result of direct tunnelling currents from inversion layer for $V_g > 0V$, where symbols are experiment data , and lines are MEDICI simulation results.



(a)



(b)

Fig.2 The device structures for overlap (a) and underlap (b) case, where S/D extensions have 5nm less diffusion in underlap case

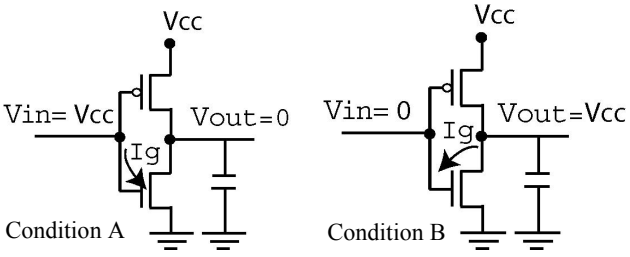
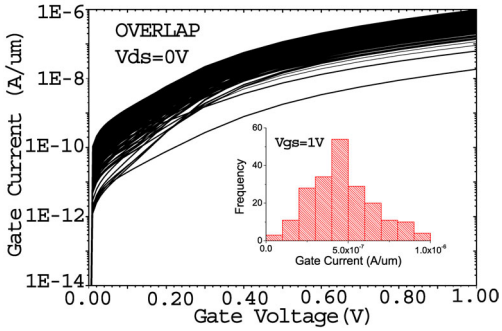
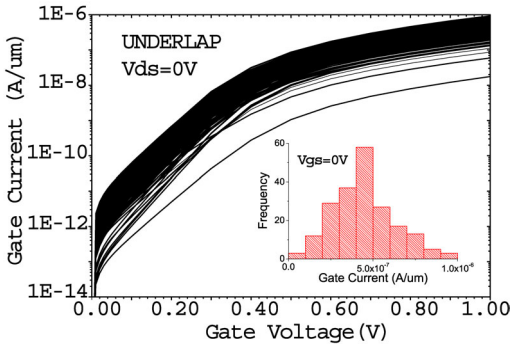


Fig.3 Two typical N MOSFET's gate leakage modes in circuit.

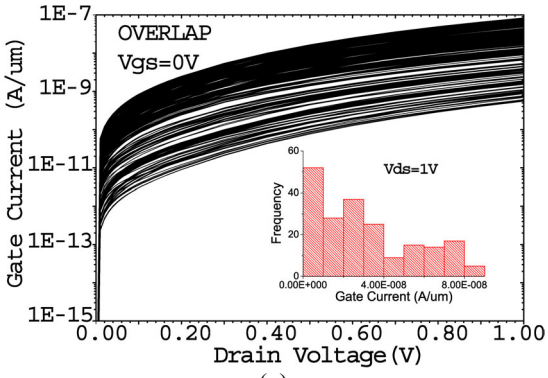


(a)

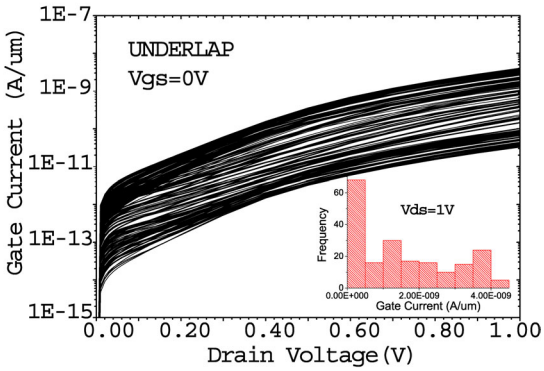


(b)

Fig.4 "Condition A"gate current characteristics from 150 macro-scopically identical 30nm nMOSFETs (a) overlap case, (b) underlap case



(a)



(b)

Fig.5 "Condition B"gate current characteristics from 150 macro-scopically identical 30nm nMOSFETs (a) overlap case, (b) underlap case