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Carrier Mobility in Multi-FinFETs with a (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching

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Introduction

Fin-type double-gate (DG) [1] MOSFETs (FinFETs) [2] have widely been investigated and its high performances e. g., the high drive current and short-channel effects (SCE) immunity have already been confirmed experimentally [3-7]. The fundamental study of the carrier mobility (μ_{eff}) on the Si-fin channel surface is essential for the accurate modeling and design for FinFET CMOS circuits. However, very few works [3, 4] on μ_{eff} in FinFETs usually with a (110) channel surface fabricated by conventional RIE processes have been reported.

This paper presents, for the first time, the experimental μ_{eff} of the hole and electron in the multi-FinFETs with a (111) channel surface fabricated by the orientation-dependent wet etching.

Fabrication process

In order to improve the Si-fin channel shape and quality, we have developed the orientation-dependent wet etching [5-8]. The etching rate for a (111) Si wafer is extremely lower than those for other planes as shown in Fig. 1. The cross-sectional SEM image of the fabricated Si-fin channels with (111)-oriented sidewalls is shown in Fig. 2, which indicates that the wet etching substantially stops at the (111) plane in the early stage of the wet etching. To examine the carrier mobility on the (111) channel surface of the Si-fins formed by the wet etching, we fabricated capacitance-measurable large multi-FinFETs, and the key fabrication processes of the multi-FinFETs are shown in Fig. 3. First, the wafers were thermally oxidized and source-drain (S-D) electrodes were patterned by EB-lithography and RIE. The S-D doping was performed by solid-phase thermal diffusion using poly boron film (PBF) and PSG for P- and N-channel devices, respectively. After the S-D doping, the same processes were adopted for the P- and N-channel devices. Figure 4 shows the plane-SEM image of the fabricated multi-FinFET with 50-fins. After the Si-fin formation, the gate oxide was directly formed on the (111) sidewalls of the Si-fins without any surface treatment. Subsequently, the n^+ poly-silicon gates were formed for both of the P- and N-channel devices. Finally, the aluminum electrodes were formed, and the devices were sintered in a forming gas ambient at 450 °C for 30 min.

Results and discussion

The cross-sectional STEM (Z-contrast) images of the fabricated P- and N-channel multi-FinFETs are shown in Fig. 5(a) and 5(b). It is noteworthy that the Si-fin channels show the perfect rectangular cross-section. The Si-fin heights (H_{fin}) are 220 and 70 nm for P- and N-channel devices, respectively. The number of Si-fin channels is designed to be 38 and 50 for the P- and N-channel devices to match drive current, so the corresponded total channel widths are W_p = 16.7 and W_n = 7 μm. The measured I_d-V_g and g_m-V_g characteristics of the fabricated P- and N-channel devices with the same gate length (L_g) of 22 μm are shown in Fig. 6. The S-slope and threshold voltage are obtained to be S_p = 63 and S_n = 78 mV/decade, and V_{tp} = -1.0 and V_{tn} = -0.2 V for the P- and N-channel devices, respectively. Almost the same drain currents in the P- and N-channel devices are observed under the same $|V_g-V_{tp,tn}|$ for different W_P and W_n as shown in Fig. 7. This indicates that the mobility of electron is larger than that of hole. The gate to channel capacitance (C_{gc}) as a function of gate voltage (V_g) was measured, and is shown in Fig. 8. The C_{gc}'s at saturation regions are exactly consisted with those as predicted. This means that the Si-fin channels were fabricated uniformly and the conductance of each Si-fin is accurately controlled by the gate bias. The carrier mobilities for hole and electron were extracted from the C_{gc}-V_g and I_d-V_d characteristics, and the results are plotted in Fig. 9. The maximum values of μ_{eff} are 165 and 284 cm^2/V-s for hole and electron, which are close to those in (111) bulk MOSFETs [9, 10]. Moreover, the obtained μ_{eff}'s are comparable or better than the reported ones in the usual FinFETs with a (110) channel surface prepared with careful surface treatments [3, 4]. This result indicates that the quality and channel surface roughness of the Si-fins by the orientation-dependent wet etching are excellent, and the developed wet etching technique is very attractive for the fabrication of high quality and ultra-thin Si-fins for FinFETs.

Conclusion

For the first time, the experimental carrier mobility in the multi-FinFETs with a (111) channel surface fabricated by the orientation-dependent wet etching has been demonstrated. The maximum hole and electron mobilities are μ_p = 165 and μ_n = 284 cm^2/V-s, and μ_n/μ_p = 1.7, which are close to those in (111) bulk MOSFETs. This indicates that the quality and channel surface roughness of the Si-fins by the wet etching are excellent. The obtained results are very useful for the modeling and design of FinFET CMOS circuits.

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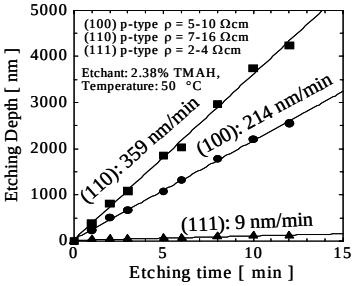

Fig. 1. Etched silicon depth versus etching time in TMAH at 50 °C. The selectivity of (110)/(111) is 40.

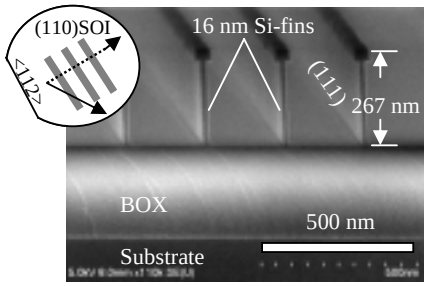

Fig. 2. SEM image of the fabricated 16-nm thick Si-fin channels. The insert is the schematic fin-patterns on the (110) SOI.

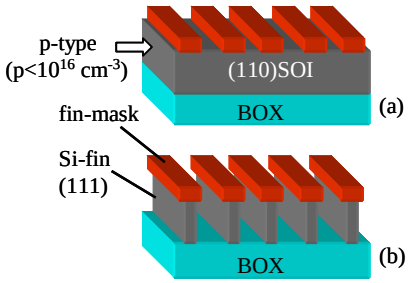

Fig. 3. Multi-fin fabrication processes. (a) fin-hard mask formation by RIE. (b) Si-fin formation by 2.38% TMAH.

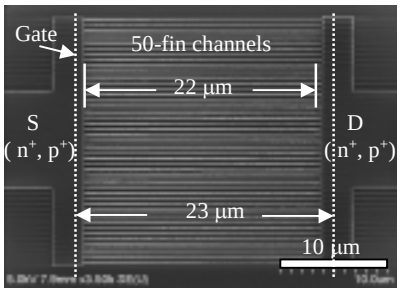

Fig. 4. Plane-SEM image of the fabricated multi-FinFET with 50-fins after the wet etching. The gate pattern is delineated by dotted lines.

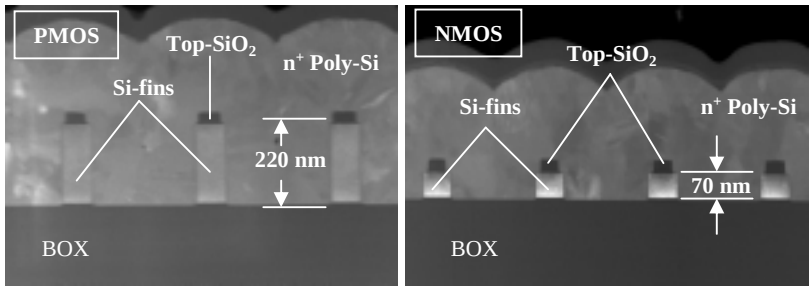

Fig. 5. Cross-sectional STEM (Z-contrast) images of the fabricated (a) P-channel and (b) N-channel multi-FinFETs. The Si-fin channels show the perfect rectangular cross-section. The Si-fin heights are 220 and 70 nm for the P- and N-channel multi-FinFETs.

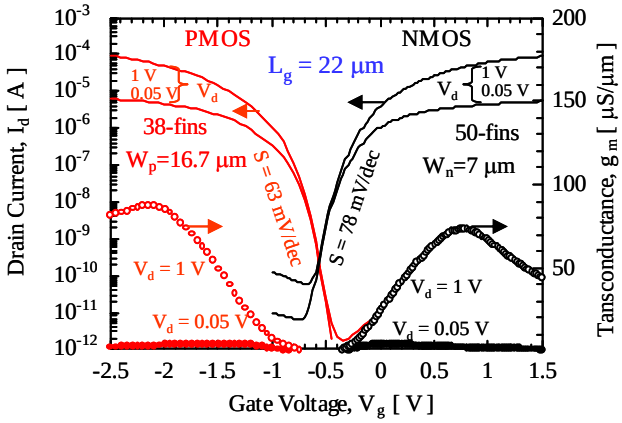

Fig. 6. I_d-V_g & g_m-V_g characteristics of the fabricated P- and N-channel Multi-FinFETs with the same gate length of 22 μm. The threshold voltages are V_{tp} = -1.0 V and V_{tn} = -0.2 V.

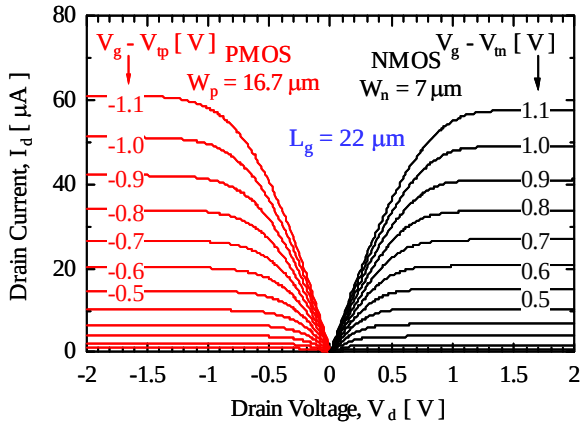

Fig. 7. I_d-V_d characteristics of the fabricated P- and N-channel multi-FinFETs with the same gate length of 22 μm.The same $|V_g-V_{tp,tn}|$ is applied for the P- and N-channel devices.

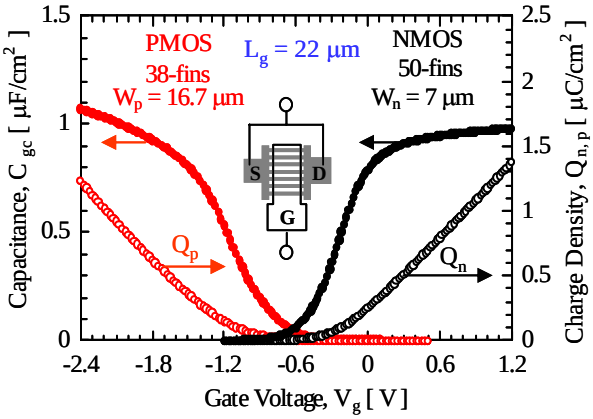

Fig. 8. Gate to channel capacitance (C_{gc}) and the charge density ($Q_{n,p}$) as a function of gate voltage. EOT for the P- and N-channel multi-FinFETs are 3.2 and 3.5 nm.

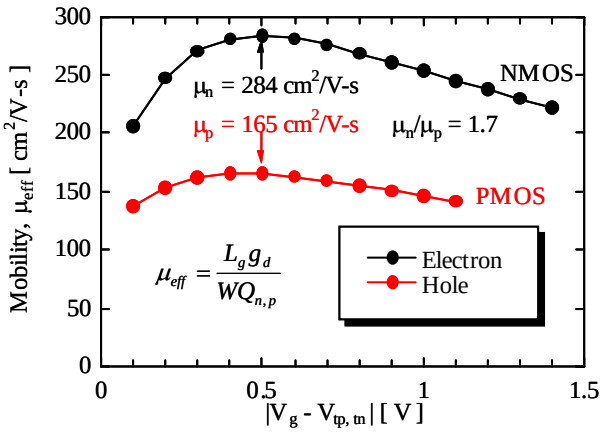

Fig. 9. Carrier mobility (μ_{eff}) for the (111) sidewalls of Si-fin channels as a function of $|V_g-V_{tp,tn}|$. The maximum values of μ_{eff} for electron and hole are μ_n = 284 and μ_p = 165 cm²/V-s, and the ratio of μ_n/μ_p is 1.7.