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Investigation and Modeling of Stress Interactions on 90 nm SOI CMOS with Various Mobility Enhancement Approaches

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Abstract

The interactions of STI stress and various mobility enhancement approaches on SOI CMOS has been systematically studied. Strong interactions between STI stress and CESL (Contact Etch Stop Layer) stress on channel mobility was observed and attributed to the amplification of CESL channel tensile-stress under the reduced LOD (Length of Diffusion). In addition, an almost completely reversed PMOS mobility-LOD trend on <110>/(100) and <100>/(100) orientated SOI wafers was observed, which is induced by the reversed polarity of piezo-resistance coefficients. On the other hand, charge pumping leakage was increased by post-gate oxide stress (such as CESL stress) only, and did not be affected by any stress prior to gate oxidation step (such as STI stress). This observation implies that processes must be integrated very carefully while pursuing any mobility enhancement scheme via post-gate oxide stress.

Introduction

MOSFET scaling has been facing serious challenges to maintain continuous performance enhancement following the ITRS roadmap [1]. Thus, mobility enhancement technologies have been actively developed including substrate biaxial stress and uniaxial process-induced stress as well as wafer orientation approaches [2,3]. Nonetheless, process stability and simplicity should be taken into serious consideration simultaneously as pushing the greatest mobility gains, especially in a foundry environment to ensure enough process and device margin for various customer products. In this study, wafer orientation and high tensile stress CESL were adopted for the simplicity in process and be compatible with conventional CMOS processes without any extra process steps or masks. Next, STI stress induced mobility improvement (or degradation) has been investigated in the past five years [4] and found that STI compressive stress improves PMOS but degrades NMOS drive current. However, the interactions between STI stress with high tensile CESL stress and wafer orientation become strong under the reduced LOD (Length of Diffusion) and have not been previously investigated. In this work, this special interaction is systematically studied and modeled on advanced 90-nm SOI CMOS. Furthermore, the accompanied reliability evaluations reveal shocking correlation between the post-gate oxide stress and the charge pumping leakage for example as applying high tensile stress CESL.

Device Preparation and measurements

SOI wafers with two channel orientations were used to fabricate high performance CMOS devices with the advanced 90-nm CMOS technology. After gate patterning for a minimum channel length of 45nm (**Fig. 1**), the transistors were integrated with shallow extension and pocket implants, followed by rapid thermal annealing. For some devices, high tensile CESL was applied after the silicidation process. To investigate CESL stress and STI stress interaction, STI stress test key was designed with various LOD dimensions and shown in **Fig. 2**. In measurements, the current and Gm were measured with HP4072A and Cascade manual probe, respectively.

Results and Discussions

Figure 3 shows that NMOS drive current is improved 8% in magnitude by high tensile stress CESL (1.2 Gpa) under the same off leakage and without any degradation of PMOS performance. In addition, the <100>/(100) wafers (<100> channel) demonstrated 10% PMOS drive current enhancement without any NMOS degradation than the <110>/(100) wafers (<110> channel). To investigate CESL stress and STI stress interaction, the mobility (represented as Gm) vs. LOD trend on control (with low tensile stress CESL) split shows only slight NMOS mobility degradation but significant PMOS mobility improvement when LOD is scaled to the minimum geometry of a 90-nm generation rule (**Fig. 4**). On the other hand, the split with high tensile stress CESL apparently improves NMOS mobility but does not degrade PMOS mobility with long LOD (regarded as without STI stress). When LOD is reduced, the high tensile CESL split shows higher NMOS but lower PMOS mobility enhancement as compared with the control samples. This is attributed to the strong interaction between STI stress and high tensile stress CESL on channel mobility, as can be evidenced from the significant difference in mobility vs. LOD trend with the high tensile stress CESL and the low tensile stress CESL. This model is illustrated schematically in **Fig.5** and confirmed by simulation (**Fig. 6**). Namely, channel tensile stress induced by CESL stress is amplified when LOD size is reduced.

Besides device performance, maintaining gate dielectric quality presents another key element in implementing high tensile CESL processes. **Fig.7** shows that gate oxide charge pumping leakages remain the same as changing LOD stress (size), but high tensile stress CESL obviously increases the charge pumping leakages on both NMOS and PMOS (**Fig. 8**). Since STI modules were implemented on CMOS prior to the gate dielectric module while the high tensile CESL processes were added to the CMOS flow after the gate dielectric steps, it is assumed that gate oxide quality will only be impacted by the post-gate oxide stress steps such as the high tensile stress CESL, but not from any stress steps before the gate oxide step. This observation implies that processes must be integrated very carefully while pursuing any mobility enhancement scheme via post-gate oxide stress.

Furthermore, the effect of channel orientation on mobility-LOD trend is depicted in **Fig. 9**, which shows that the <100> channel direction is largely insensitive to STI stress similar to previously reported results by T. Okagaki [5]. However, PMOS trends in the <110> and <100> channel directions are quite different. A PMOS degradation with smaller LOD is observed for the first time in 45nm channel-length devices. In order to understand the mechanism, the longitudinal and transverse piezo-resistance coefficients of <110> and <100> channels are listed in **table 1** for surface carrier concentrations around 1E17 and 1E18 atoms/cm^3 where the latter should be applied to short channel CMOS due to its strong pocket implantations overlapping each other [6]. The reverse trend is mainly attributed to the reversed polarity in longitudinal piezo-resistance coefficients when channel dopant concentration increases to 1E18 atoms/cm^3. The transverse piezo-resistance coefficient is relatively small and, thus, does not play a significant role in mobility.

Conclusion

The interaction of STI stress with various mobility enhancement approaches is systematically studied and reported. A strong interaction between STI stress and CESL stress to induce markedly different in STI LOD mobility trends was found. Additionally, an almost completely reversed PMOS LOD trend on <110> and <100> channel SOI wafers was observed and be attributed to the reversed polarity of piezo-resistance coefficients. On the other hand, charge pumping leakage is affected only by post-gate oxide stress and not by any pre-gate oxide stress step. This observation implies that processes must be integrated very carefully while pursuing any mobility enhancement scheme via post-gate oxide stress.

References

[1] http://public.itrs.net/Files/2003ITRS/Home2003.htm .
[2] K. Mistry, *et al.*, *VLSI Symp.*, 2004.
[3] T. Sanuki, et al., *IEDM*, 2003.
[4] G. Scott, et al., *IEDM*, 1999.
[5] T. Okagaki, *et al.*, *VLSI Symp.*, 2004.
[6] K. Matsuda, *et al.*, J. Appl. Phys. 73 (4), 1993.

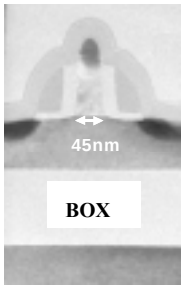

Fig. 1 Cross-sectional TEM view of SOI wafer with 45 nm channel length.

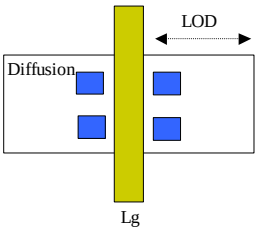

Fig. 2 Test key design of LOD effect, with various LOD dimensions.

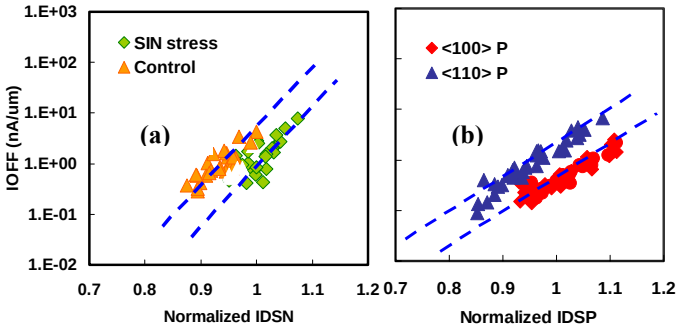

Fig. 3 Mobility enhancement approaches demonstrated 8% and 10% current gain by (a) high tensile stress CESL (b) <100>/(100) wafer on N/PMOS, respectively.

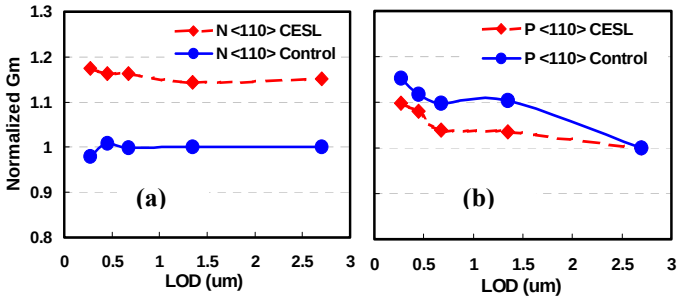

Fig. 4 The LOD mobility trend of high and low tensile stress CESL on <110>/(100) SOI wafer, (a) NMOS, (b) PMOS.

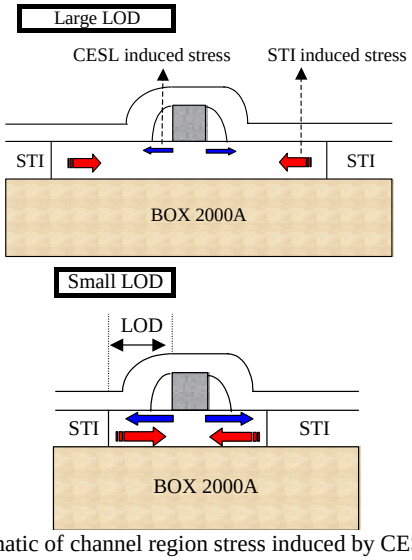

Fig. 5 Schematic of channel region stress induced by CESL and STI. Channel tensile stress induced by CESL stress is amplified when LOD size is reduced.

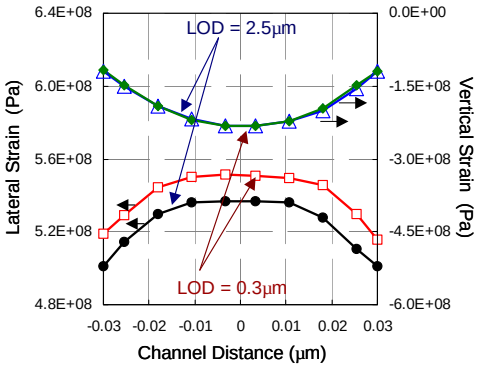

Fig. 6 Simulation data of CESL induced channel stress on LOD = 2.5 um and 0.3 um, STI stress was assumed to be negligible in this simulation.

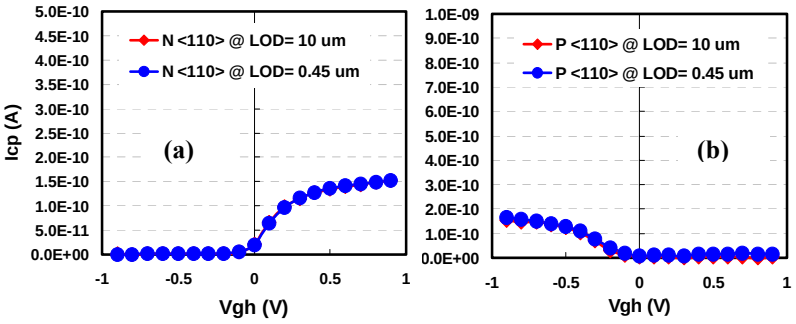

Fig. 7 (a) NMOS, (b) PMOS charge pumping current stays the same while changing LOD dimension on <110>/(100) orientated SOI wafers.

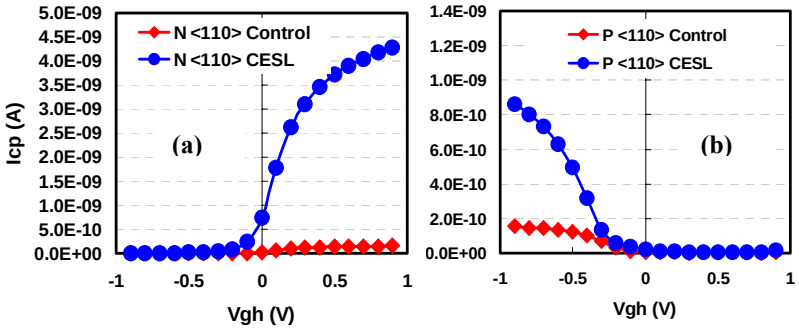

Fig. 8 High tensile stress CESL induced higher charge pumping current on both (a) NMOS and (b) PMOS.

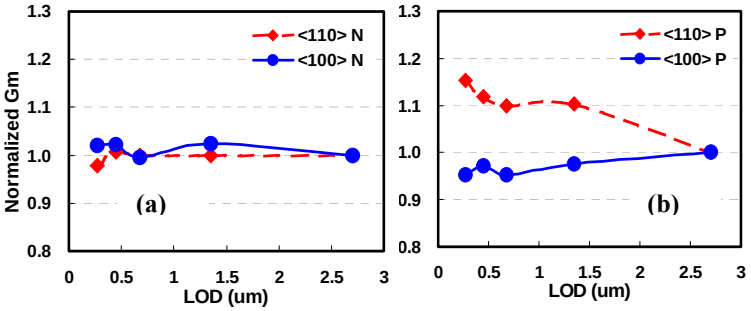

Fig. 9 (a) NMOS, (b) PMOS LOD mobility trend of <110>/(100) and <100>/(100) orientated SOI wafers.

Table. 1 Piezo-resistance coefficient varied with channel direction and surface concentration.

Channel	<100>		<110>	
(~1E18 atoms/cm^3)	πL	πT	πL	πT
N-Si	-65	33	-22	-10
P-Si	-4	3	48	-49

Channel	<100>		<110>	
(~1E17 atoms/cm^3)	πL	πT	πL	πT
N-Si	-102	53	-32	-18
P-Si	7	-1	72	-66