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MEMS 3-D Stacked RF Transformers Fabricated by 0.18 μm MS/RF CMOS technology With Improved Power Loss and Noise Figure Performances

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Abstract - Selective removal of the silicon underneath the transformers in MS/RF integrated circuits based on inductively-coupled-plasma (ICP) deep trench technology is demonstrated. A 20.6 dB improvement in isolation (from -40.4 dB to -61dB) was achieved for a dummy open device after the backside ICP dry etching. A 102% increase in Q-factor (from 4.96 to 10) was achieved at 5.2 GHz for an interlaced fully symmetrical stacked transformer with turn ratio of 1:1 after the backside ICP dry etching. In addition, for a 3-D stacked transformer with turn ratio of 1:2 after the backside ICP dry etching, a 40% increase in Q-factor (from 2 to 2.8), a 14.1% increase in maximum power gain G_{Amax} (from 0.461 to 0.526), and a 17.2% reduction in minimum noise figure NF_{min} (from 3.37 dB to 2.79 dB) are obtained at 2 GHz. These results show the CMOS process compatible backside ICP etching technique is very promising for system-on-a-chip (SOC) applications.

I. Introduction

Recently, RF silicon Bipolar, CMOS, and BiCMOS processes have become more and more popular for RF-IC's operated in the 5 GHz band or even higher frequency bands [1]-[2]. However, the quality factor (Q-factor) and noise figure (NF) performances of monolithic RF transformers fabricated on normal silicon substrates (~ 700 μm) are not satisfactory up to now mainly due to the silicon substrate loss. In addition, the NF_{min} of a transformer is an index of the power loss of the device. In the design of low-voltage-supply transformer-feedback low-noise-amplifiers (LNAs) [3] and voltage-controlled-oscillators (VCOs) [4], the NF performances of transformers are crucial for the overall NF performance of the LNAs and the phase noise performance of the VCOs. Therefore, in this work, the CMOS compatible backside ICP deep trench technology, which selectively removes the conductive silicon substrate underneath the transformers completely, is demonstrated.

II. Experimental Results and Discussions

A complete set of 3-D stacked RF transformers were implemented by a 0.18 μm MS/RF CMOS technology provided by the commercial foundry TSMC. All the transformer chips were gone through the proposed backside ICP dry etching. Fig. 1(a) and 1(b) show the front-side die photo and the 3-D schematic diagram of a stacked transformer (K4) with turn ratio of 1:2. Fig. 1(c) shows the bask-side die photo of a chip which includes 8 transformers. Transformer K4 is indicated by a dashed circle. As can be seen, the exposed front-side on-chip transformers are visible to the naked eye and the sidewalls of the "drilled" or micro-machined holes are virtually vertical. Compared with the traditional backside wet bulk micromachining, the dry ICP etching has the advantages of forming vertical sidewalls and being fully CMOS process compatible since it is a standard processing technique in modern CMOS technology.

Fig. 2(a) shows the measured isolation (S_{21}) of a dummy open pad device. As can be seen, a 20.6 dB improvement in isolation (from -40.4 dB to -61dB) was achieved. Fig. 1(b) shows the measured quality factor of the primary coil (Q1) of transformers K9 and K4. K9 is an interlaced fully symmetrical stacked transformer with turn ratio 1:1. A 102% increase in Q1 (from 4.96 to 10) was achieved at 5.2 GHz for transformer K9 after the backside ICP dry etching. A 40% increase in Q-factor (from 2 to 2.8) was achieved at 2 GHz for transformer K4 after the backside ICP dry etching.

Fig. 3 shows the small-signal equivalent circuit model of a transformer. The extracted equations of the equivalent inductance of the primary coil $L_{s1\text{-}eff}$, the equivalent resistance of the primary coil $R_{s1\text{-}eff}$, Q-factor of the primary coil (Q1), Q-factor of the secondary coil (Q2), mutual resistive coupling factor k_{Re}, and mutual reactive coupling factor k_{Im} from the measured S-parameters are also shown. Clearly, reducing substrate loss leads to a larger Q1 and Q2, i.e. a smaller x, and therefore, a higher G_{Amax} and a lower NF_{min}. This explains why ICP backside dry etching can improve the Q_1, Q_2, G_{Amax} and NF_{min} of transformers effectively.

Fig. 4(a) shows the measured K_{Re} and K_{Im} of transformer K4. High K_{Im} of 0.94 was achieved at 2 GHz. Fig. 4(b) shows the measured G_{Amax} and NF_{min} of transformer K4. The improvement in G_{Amax} (14.1%) and NF_{min} (17.2%) was attributed to the reduction of the silicon substrate loss by our proposed backside ICP dry etching. Fig. 4(c) shows the measured K_{Re} and K_{Im} of transformer K9. Perfect magnetic coupling k_{Im} of 1 was achieved. In addition, very good G_{Amax} of 0.9 and NF_{min} of 0.482 were achieved at 5.2 GHz for transformer K9 after backside ICP dry etching (not shown here). This means the interlaced fully symmetrical stacked transformer structure can be used to implement ultra-low-loss 5-GHz band transformers/baluns and even 30-100 GHz millimeter transformers/baluns.

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Structure	Metal Width (μm)	Metal Space (μm)	Turn Number	Turn Ratio	Outer Dimension (μm×μm)	Inner Dimension (μm×μm)
Stacked 3D	10	10	4	1:2	240×240	60×70

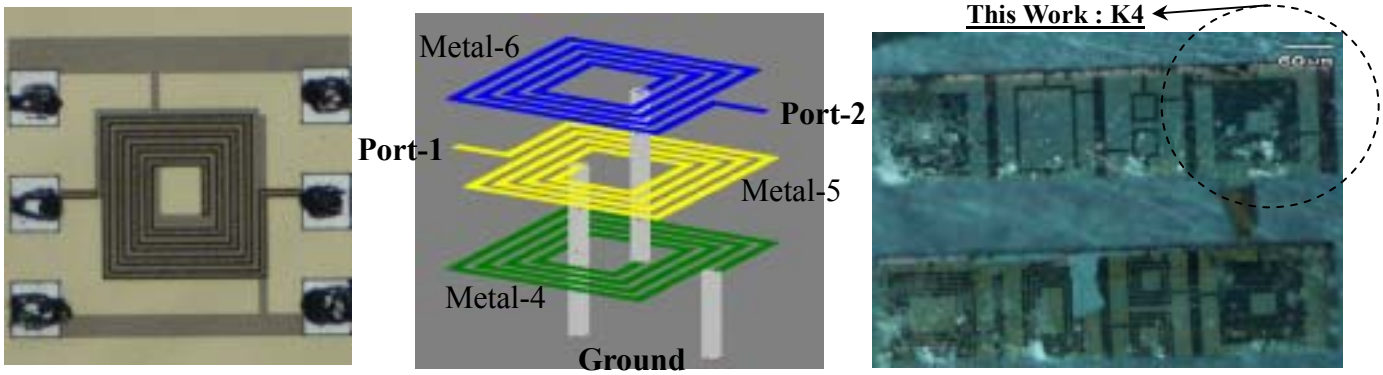

Fig. 1 (a) Top-view die photo, (b) 3-D schematic diagram, and (c) bask-side die photo of the stacked transformer with turn ratio of 1:2 studied in this paper.

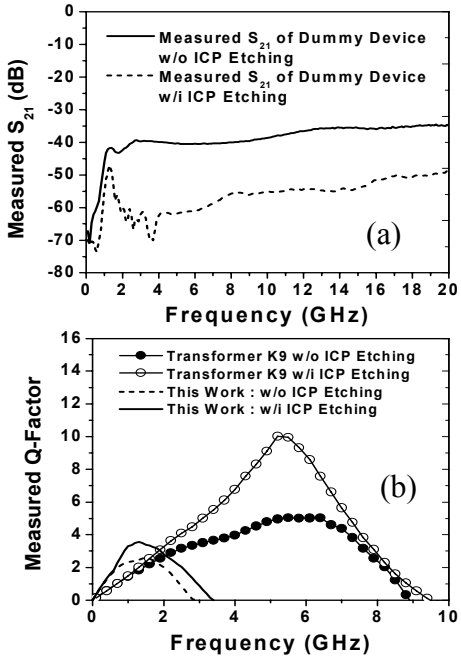

Fig. 2 Measured (a) isolation (S_{21}) of dummy open device, and (b) Q1 of transformers K4 and K9 with and without ICP dry etching.

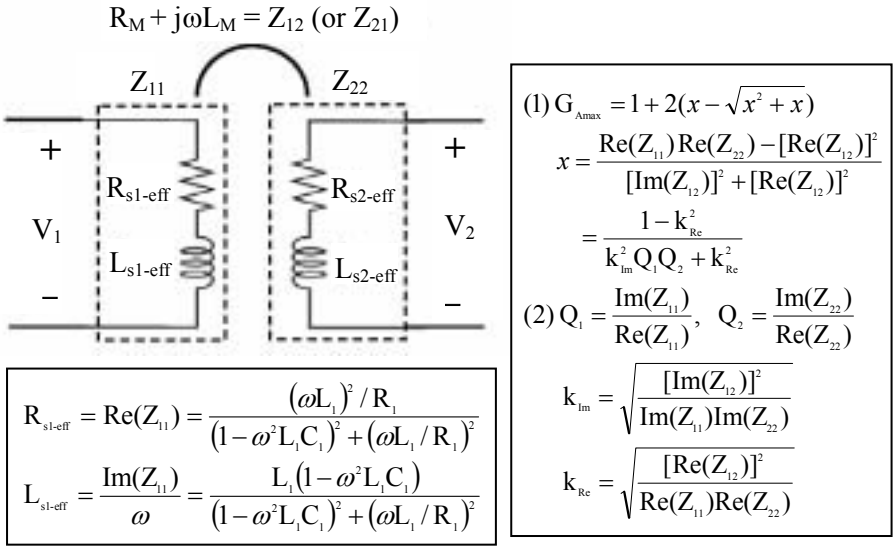

Fig. 3 Small-signal equivalent circuit model of a 3-D stacked transformer. The extracted equations of $L_{s1\text{-}eff}$, $R_{s1\text{-}eff}$, Q-factor of primary coil (Q1), Q-factor of secondary coil (Q2), k_{Re}, and k_{Im} from the measured S-parameters are also shown.

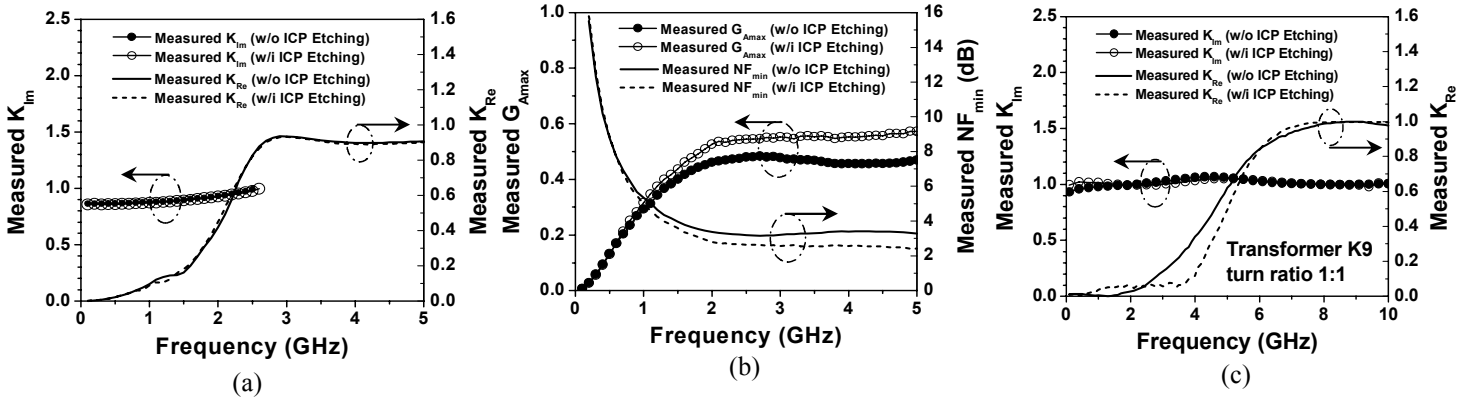

Fig. 4 Measured (a) K_{Re} and K_{Im}, and (b) G_{Amax} and NF_{min} of the stacked transformer K4 with turn ratio of 1:2. Measured (c) K_{Re} and K_{Im} of an interlaced stacked transformer with turn ratio of 1:1.