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Mobility Modulation Technology Impact on Device Performance and Reliability for <100> sub-90nm SOI CMOSFETs

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1. Introduction

<100> channel orientation substrate and high tensile stress gate capping layer (GC liner-SiN) have been adapted for the mobility improvement of CMOSFETs [1-4]. There are few reports studying the effects of GC liner-SiN film thickness on device's characteristic and reliability. In this work, the impacts of high tensile stress GC liner-SiN thicknesses on device performance and hot-carrier induced degradations for 90nm PD-SOI CMOSFETs were investigated. We also inspect the stress come from GC liner-SiN and STI edge impact on device characteristic using the length of diffusion (LOD) check.

2. Experiments

PD-SOI CMOSFETs were fabricated on <100> channel orientation SOI substrate based on advanced 90nm CMOSFETs process with 200nm buried oxide layer (BOX) and 40nm Si layer using STI isolation technology. Sub-90nm devices were fabricated with different thicknesses of high tensile stress GC liner-SiN layer (700A, 1100A) and LOD (0.45μm~4.5μm). Device measurements and hot-carrier stressing were performed on probe station using various drain voltages (V_D=0~1.4V), and various gate voltages (V_G=0~1.4V) with 100 minutes hot-carrier stress time.

3. Results

Figure 1 shows the control methods of stress orientation. High stress liner-SiN induces a tensile stress in channel region, and STI induces a compressive one. From previous studies [1], it is found that <100> channel orientation substrate will enhance the mobility of pMOSFET and channel tensile stress induced by GC liner-SiN layer will enhance the mobility of nMOSFET; besides, a thicker (140A) liner-SiN layer will induce higher stress and improve the device performance[2]. However, in this work we found that thick GC liner-SiN layer (1100A) have no apparent improvement on device performance. The threshold voltage (V_{TH}) roll-off of 90nm BC-SOI nMOSFETs was shown in Fig. 2. It is obvious that devices with 700A GC liner-SiN layer have a lower V_{TH} and a smaller V_{TH} roll-off than devices with 1100A GC liner-SiN layer. And devices with 700A GC liner-SiN also possess smaller subthreshold swing and better I_{on}-I_{Off} characteristics than 1100A ones (Fig.3 and 4). The I_D-V_D characteristics of 90nm BC and FB-SOI nMOSFETs are shown in Fig. 5. For body-tied device (BC-SOI), it is apparent that devices with GC liner-SiN possess larger drain current density (I_D) than conventional devices (SiN 380) does, and I_D in 700A device is much larger than that in 1100A one. Compared with BC-SOI, I_D of FB-SOI is high because of the floating body effect, and 700A devices possess the highest I_D. There are no apparent different between conventional (SiN 380) and 1100A GC liner-SiN devices. Same tendency was found in G_m characteristic (Fig. 6). In this work, larger mobility can be found on device with 700A GC liner-SiN. Figure 7 shows the I_D-V_D characteristics of 90nm BC-SOI nMOSFETs after 100min hot-carrier stressing. Because device's V_{TH} shifted after hot-carrier stressing, as shown in Fig. 8; thus, I_D rises apparently after hot-carrier stressing first and then degrades finally especially in 1100A device. Similar tendency was found on device's G_m characteristic. It is apparent that devices with 700A GC liner-SiN are more stable (I_D and G_m) after hot-carrier stress. It is presumably that thicker GC liner-SiN layer (1100A) will induce larger tensile stress and cause more serious damage to lattice structure, resulting in more serious hot-carrier induced device degradations (HCIDD). Figure 9 shows that lower V_{TH} was found on 90nm BC-SOI nMOSFETs with 1100A GC liner-SiN layer. We believed that more holes were trapped in the Si-SiO_2 interface during the hot-carrier stressing, thus lowering the V_{TH} and raising the I_D. Besides, hot-carrier induced V_{TH} variation in devices with 700A GC liner-SiN is more stable than that in devices with 1100A GC liner-SiN. In order to inspect the stress come from GC liner-SiN film and STI edge impact on device performance, various length of diffusion (LOD 0.45μm~4.5μm) was used for comparison. The insert shows the test structure of LOD. Figure 10 shows the I_D-V_D of 700A GC liner-SiN SOI nMOSFETs with various LOD. Increasing the LOD will decrease the compressive stress caused by shallow trench isolation (STI), and increase tensile stress caused by high stress GC liner-SiN. Thus I_D increases apparently with LOD increases. Same tendency was found in the G_m characteristic for mobility check, as shown in Fig. 11. No V_{TH} shift was found while LOD changed. For pMOSFETs, It had been known that the major factor of mobility improvement is <100> channel orientation substrate [1]. In this work, it is found that for 90nm BC-SOI and FB-SOI pMOSFETs, even with various GC liner-SiN thicknesses, there is no apparent change on device characteristic (I_D and G_m), as shown in Fig. 12 and 13. Therefore, the effect of GC liner-SiN for SOI pMOSFETs is not apparent. Figure 14 shows the G_m characteristics for 90nm BC-SOI pMOSFETs with different stress GC liner-SiN thicknesses before and after 100min hot-carrier stressing; the inserts show the hot carrier induced I_D degradation. Similar tendency of hot-carrier induced device degradations was found for both stress GC liner-SiN device (700A, 1100A). The G_m characteristics degraded apparently just after 20min hot-carrier stressing and had a V_{TH} shift, then very serious device breakdown was found. Compared with nMOSFETs, the variations of pMOSFETs characteristics were sensitive; thus pMOSFETs is easy to be degraded and lost the MOSFET characteristics especially after the hot-carrier stressing. Table I summarizes the mobility modulations induced by various stress items. It is found that the stress technology impacts of device performance for mobility improvement are different for n and pMOSFETs in respectively. For nMOSFETs, thin GC liner-SiN layer (700A) has apparent improvement on device performance than thick one (1100A) does. For pMOSFETs, the GC liner-SiN doesn't show apparent impact on device's performance.

4. Summary

In this work, for 90nm PD-SOI CMOSFETs on <100> Si substrate, the impacts of high tensile stress GC liner-SiN thicknesses on device performance and hot-carrier induced degradations were investigated. For nMOSFETs, devices with 700A GC liner-SiN possess apparent mobility enhancement and hot-carrier reliability immunity than devices with 1100A GC liner-SiN do. We believed that thicker GC liner-SiN (1100A) will induce large stress defects and makes damage to the device's channel lattice structure, thus degrading device characteristics. For pMOSFETs, the effects of high tensile stress GC liner-SiN thicknesses on device performance are not apparent. The major factor of mobility improvement is <100> channel orientation Si substrate. It is necessary to optimum high tensile stress GC liner-SiN technology to enhance pMOSFETs reliability.

Acknowledgement

The National Science Council of Taiwan, R.O.C., under Contract NSC 93-2215-E-390-001 and NSC 93-2215- E-006-005, supported this work.

References

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[2] K. Goto, *et. al*, *in IEDM Tech. Dig.*, 2004, p. 209
[3] S. Pidin, *et. al*, *in IEDM Tech. Dig.*, 2004, p. 213
[4] T. Ghani, *et. al*, *in IEDM Tech. Dig.*, 2003, p. 11.6.1

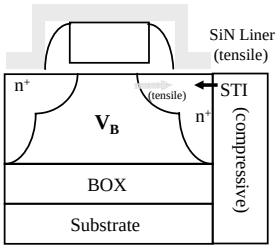

Fig. 1. The stress item in MOSFET channel region. High stress liner-SiN induces a tensile stress, and STI induces a compressive one.

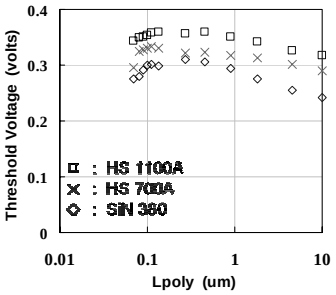

Fig. 2. V_{TH} of BC-SOI nMOSFETs with various stress GC liner-SiN layer.

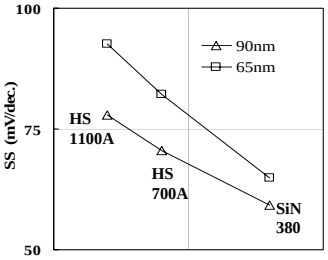

Fig. 3. Subthreshold Swing of BC-SOI nMOSFETs with various stress GC liner-SiN layers.

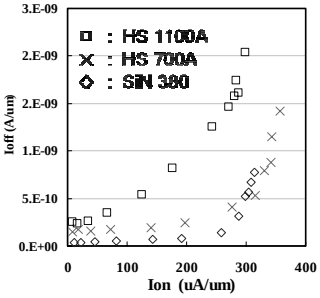

Fig. 4. I_{ON}-I_{OFF} characteristics of BC-SOI nMOSFETs with various stress GC liner-SiN layer.

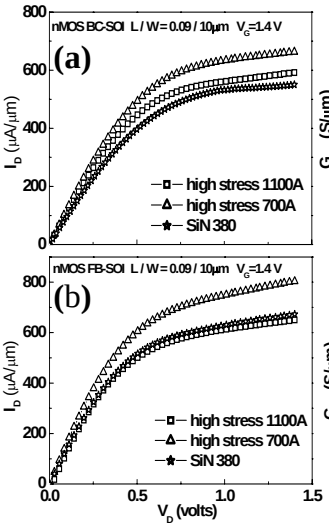

Fig. 5. I_D-V_D of 90nm (a)BC-SOI (b)FB-SOI nMOSFETs with various stress GC liner- SiN thicknesses.

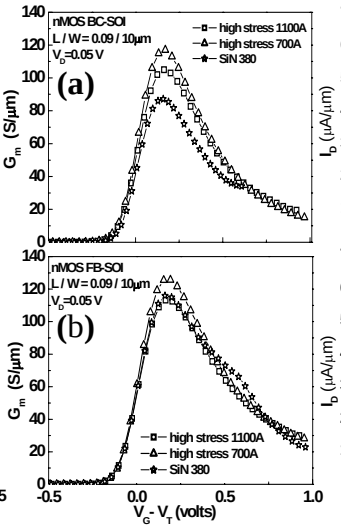

Fig. 6. G_M of 90nm (a)BC-SOI (b)FB-SOI nMOSFETs with various stress GC liner-SiN thicknesses.

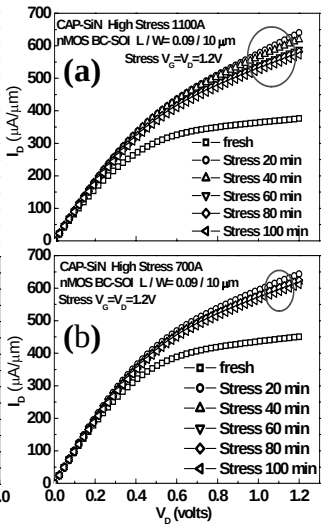

Fig. 7. I_D-V_D of 90nm BC-SOI nMOSFET with (a) 1100A (b) 700A high stress GC liner-SiN after 100 min hot carrier stressing.

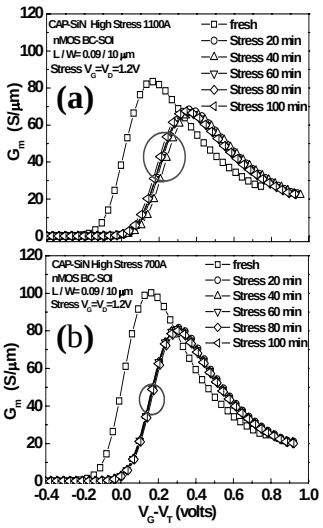

Fig. 8. G_M of 90nm BC-SOI nMOSFET with (a) 1100A (b) 700A high stress GC liner-SiN after 100 min hot carrier stressing.

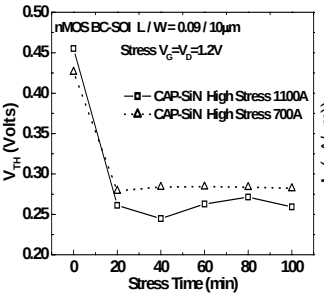

Fig. 9. V_{TH} variation of 90nm BC-SOI nMOSFET with different high stress GC liner-SiN after 100 min hot carrier stressing.

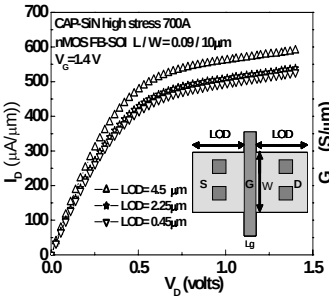

Fig. 10. I_D-V_D of 90nm FB-SOI nMOSFETs with various LOD. The insert shows the design of LOD.

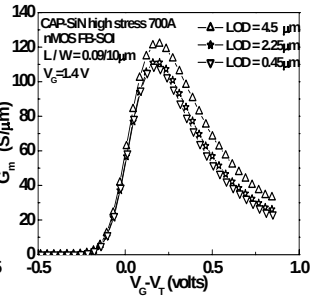

Fig. 11. G_M of 90nm FB-SOI nMOSFETs with various LOD.

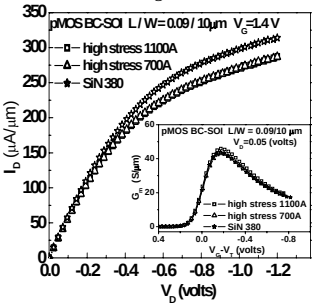

Fig. 12. I_D-V_D of 90nm BC-SOI pMOSFETs with various stress GC liner-SiN thicknesses. The insert shows the G_M characteristics.

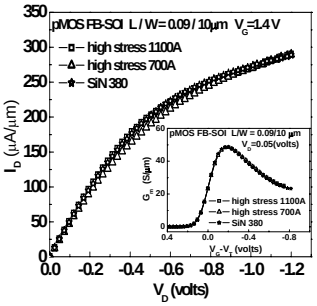

Fig. 13. I_D-V_D of 90nm FB-SOI pMOSFETs with various stress GC liner-SiN thicknesses. The insert shows the G_M characteristics.

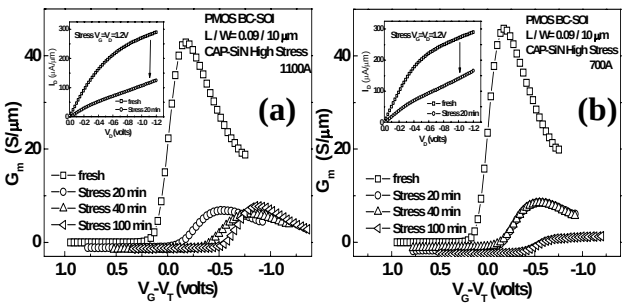

Fig. 14. G_M characteristics of 90nm BC-SOI pMOSFET with (a) 1100A (b) 700A high stress GC liner-SiN after 100 min hot carrier stressing. The insert shows the I_D-V_D characteristics. Both devices show unstable characteristics during hot-carrier stressing process.

Stress item	nMOS		pMOS
<100> channel	→		↗
GC Liner-SiN	700A ↗ +	1100A ↗	→
LOD	↗		↗ −
HCID D	700A stable	1100A unstable	All unstable

Table I. The summary of mobility modulations induced by various stress item.