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The DC Performance of Nanometer MOSFETs: Targets Versus Reality

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1. Introduction

To continue successful MOSFET scaling during the next 10 years, transistors scaled toward 10-nm gate length with improved performance are needed [1]. Operating MOSFETs with 5...10nm gates have already been fabricated [2-3]. Their DC performance, however, is still not sufficient to meet the ITRS targets. Two key DC performance parameters are the on-current I_{on} and the off-current I_{off}. For downscaled MOSFETs, I_{on} is required to increase considerably under simultaneously decreasing supply voltage levels, and under the condition that I_{off} does not exceed a tolerable upper limit. A recent study based on the 2001 ITRS revealed that it generally becomes questionable whether the required performance improvement can be accomplished for extremely scaled MOSFETs [4].

The aim of the present paper is to critically assess the DC performance of recently reported nanometer MOSFETs, to clarify to what extend the ITRS targets (in particular the I_{on}-targets for n-channel high-performance logic transistors) are met, and to discuss reasonable ways to improve transistor performance. To this end, we first examine the on-currents of experimental MOSFETs reported recently. Based on the observed trends, the transconductance required to meet the I_{on}-targets is estimated and compared to that of experimental transistors. Finally, options to improve the on-current and transconductance of nanometer MOSFETs are discussed.

2. The I_{on}-I_{off} Performance of Nanometer MOSFETs

To ensure a meaningful assessment of transistor DC performance, first a reasonable benchmark criterion based on the ITRS specifications is to be defined. Our criterion is the on-current a transistor is able to deliver for the supply voltage condition specified in the ITRS for the transistor's gate length ***and*** under the constraint that the I_{off}-target is just met. If for a certain transistor the reported *I-V* characteristics are given for supply voltages different from the ITRS specifications or if the off-current is different from the I_{off}-target, the *I-V* characteristics are appropriately adjusted to extract the on-current according to the criterion defined above.

The *I-V* characteristics of a large number of experimental nanometer MOSFETs have been compiled from the literature [5]. Figure 1 shows the extracted on-currents as a function of gate length together with the ITRS I_{on}-targets. Several alarming facts concerning the current drive capability of nanometer MOSFETs can be seen. (a) While in the gate length range between 65 and 35 nm the best transistors show a continuous increase of I_{on} for decreasing gate length, below 35nm the on-currents decline rapidly. (b) Below 30nm no transistor reported so far, including advanced MOSFETs structures (e.g., strained Si and multiple gate MOSFETs), meets the ITRS I_{on}-target. (c) The gap between the targets and the experimental on-currents widens dramatically towards 10-nm gate length.

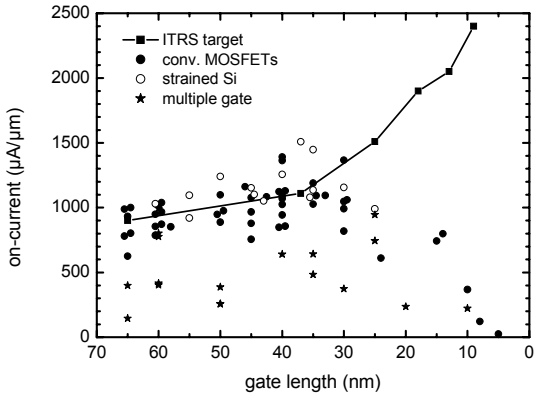

Fig. 1 Extracted on-currents of experimental MOSFETs as a function of gate length.

It should be noted that several transistors from Fig. 1, especially in the sub-30nm range, have been fabricated to introduce new innovative technology concepts and that their designs are still not optimized. Nevertheless, the trend clearly shows that much work is to be done to improve the on-currents of sub-30 nm MOSFETs.

3. Transconductance Issues

Figure 2 shows that the I_D-V_G characteristics of a MOSFET can be divided into three gate voltage regions designated by ΔV_{G1}, ΔV_{G2}, and ΔV_{G3}. The ΔV_{G1} region extends from V_G=0 to the threshold voltage V_{Th} (i.e., the gate voltage at which the drain current becomes 5×10^{-7}A/μm × width/length). The lower bound of the ΔV_{G3} region is obtained by extrapolating the linear portion of the I_D-V_G characteristics to zero I_D. Finally, we have the intermediate transition region ΔV_{G2} between regions ΔV_{G1} and ΔV_{G3}.

An inspection of the compiled I_D-V_G characteristics reveals that for most transistors with gate lengths down to 15nm the ΔV_{G1}, ΔV_{G2}, and ΔV_{G3} regions account for about 20%, 10%, and 70%, respectively, of the supply voltage V_{DD} specified in the ITRS for the transistor's gate length. As an example, the inset of Fig. 3 shows the extracted ΔV_{G3} as a function of gate length.

Based on the above considerations, we now estimate the minimum terminal transconductance, g_m, needed to obtain

an on-current equal to the I_{on}-target by $g_m = I_{on}/\Delta V_{G3}$. To this end, we make the following rather optimistic assumptions: (a) The 20:10:70 split of V_{DD} for ΔV_{G1}, ΔV_{G2}, and ΔV_{G3} holds for all gate lengths. (b) The drain current shows a linear V_G-dependence up to V_G=V_{DD} (i.e., the frequently observed sub-linear I_D-V_G dependence for gate voltages approaching V_{DD} is neglected).

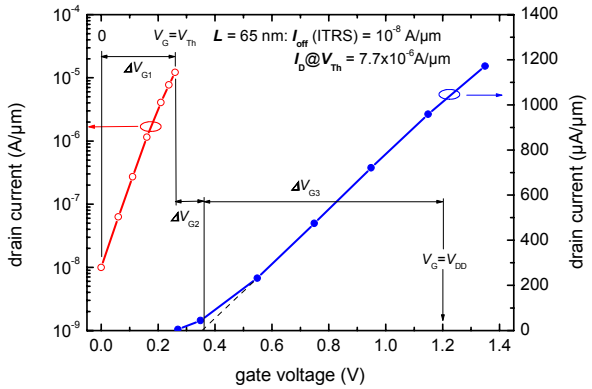

Fig. 2 Three regions of the I_D-V_G characteristics of a MOSFET.

Figure 3 shows the transconductance estimated as discussed above, together with the transconductance of experimental nanometer MOSFETs as a function of gate length. It can be seen that transistors with gate lengths of 25, 18, and 13nm (which correspond to the hp65, hp45, and hp32 technology nodes of the ITRS) should possess a transconductance of at least 1960, 2715, and 3250µS/µm, respectively. Unfortunately, no experimental transistor reported so far for these gate length levels fulfills this requirement.

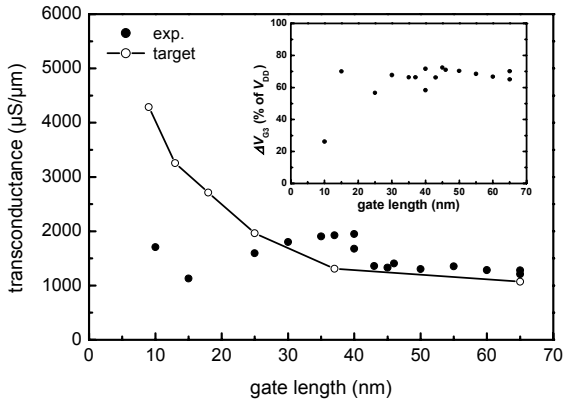

Fig. 3 Transconductance needed to meet the ITRS I_{on}-target and transconductance of experimental MOSFETs as a function of gate length. Inset: extracted ΔV_{G3} (in % of V_{DD}) of experimental MOSFETs vs. gate length.

It is unlikely that the subthreshold and near-threshold behavior of sub-30nm MOSFETs can be improved compared to transistors with 35-50nm gate length. In other words, we cannot expect that the share of ΔV_{G1} and ΔV_{G2} in V_{DD} will decrease and that of ΔV_{G3} will increase. Instead, it has to be assumed that a gate voltage swing of no more than 70% V_{DD} is available to change the drain current from almost zero to the required I_{on}. Therefore, in the following we discuss several issues related to question: How can we get a high transconductance, and thus a high on-current with a V_G swing limited to 70% of V_{DD}.

Crucial for a high terminal transconductance is a high intrinsic transconductance, g_{mi}, combined with low parasitic series resistances. If we assume a fictive 18-nm transistor with the required g_m of 2715 µS/µm and a source series resistance R_S of 67.5Ω-µm (this corresponds to the ITRS target for R_S), the intrinsic transconductance is about 3325 µS/µm according to $g_{mi} = g_m/(1-g_m \times R_S)$. For an R_S 2× and 4× the ITRS target, intrinsic transconductances of 4285 and over 10 000 µS/µm, respectively, would be necessary!

Among the options to achieve the required high g_m below 30nm are: (a) the use of channel materials with enhanced transport properties (e.g., strained Si), and (b) to employ transistor designs which result in higher inversion layer sheet densities n_S combined with an excellent controllability of n_S, i.e., high $\Delta n_S/\Delta V_G$. It has been shown that strained Si leads to higher carrier mobilities and higher drain currents compared to conventional bulk Si. The expected on-current enhancement of about 10-30% is, however, not sufficient to meet the ITRS targets toward 10nm gate length (see Figs. 1, 3). Therefore, currently we believe that option (b) shows larger potential.

Increased inversion layer sheet densities and enhanced $\Delta n_S/\Delta V_G$ are possible by replacing polysilicon gates by metal gates and by gate dielectrics with a very small equivalent oxide thickness, *EOT*. While the effect of metal gates is expected to be limited, the introduction of high-κ dielectrics can lead to smaller *EOT* and considerably increased n_S and $\Delta n_S/\Delta V_G$. Here it is important that the positive effect of the high-κ dielectric is not compensated by a degradation of the transport properties of the inversion channel. This is still a technological challenge.

4. Conclusions

The DC performance of experimental nanometer MOSFETs has been analyzed. It has been shown that so far the I_{on} and g_m performance of sub-30nm transistors is not sufficient to meet the ITRS targets. Options to improve the DC performance include the minimization of series resistances, the enhancement of the channel transport properties, as well as the increase of the channel sheet density and its controllability by the gate voltage. Regardless of the existing problems, currently it seems as if the decrease of *EOT* by introducing high-κ dielectrics will be the most effective option to increase the transconductance and the on-current.

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