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A High Performance Embedded 60nm Gate Length CMOSFET with Novel Strained Silicon Process

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Abstract:

Managing intrinsic mechanical stress is vital to achieve high performance and robust reliability in advanced CMOS technologies. Process induced strain effect dominates as device dimension shrinks. For example, STI induced strain in the channel region can markedly impact the drive current of both NMOS and PMOS devices. Many papers have reported on the stress of nitride liner, which is traditionally used as a contact etch stop layer, and its impact on device performance. However, very few studies have dealt with the stress of LDD spacers and its effect on transistor characteristics. In this report high performance 60nm devices are integrated into a 130nm baseline logic. Aggressive scaling of gate length and gate oxide thickness is implemented in order to improve the product speed at same leakage level. In addition, mechanical stress engineering techniques were applied to LDD spacers and contact nitride liner to further enhance the transistor performance.

Devices are fabricated on 300nm (100) silicon substrate. Figure 1 shows the cross-section of a 60nm MOSFET. Shallow trench isolation and well profiles are similar to those used in the baseline logic. 193nm lithography combined with optical proximity correction (OPC) are adopted to improve the resolution and process window. Gate dielectric is scaled to 1.6nm EOT to improve the device drive current and required overdrive capability. Nitridation of the Gox growth process is optimized to achieve high drive current without degrading gate leakage and channel mobility. Delicate optimization of source/drain extension, halo implants and subsequent spike activation anneal are indispensable to prevent the increase of parasitic junction capacitance and degradation of channel mobility. Cobalt salicide is formed in the poly and source/drain regions. Copper wiring with low-K dielectric are used to reduce BEOL metal Rs and interconnect RC.

Experiments were performed on two types of films on LDD spacers: 1) strong compressive (SCS), 2) compressive (MCS), and two types of nitride liner film: 1) strong compressive (SCN), 2) neutral (NCN),. Figure 2 and 3 show the on-state drive current versus off-state leakage current characteristics of NMOS and PMOS measured at 1.2V. The strong compressive LDD spacer film in conjunction with neutral nitride liner film did not degrade the NMOS performance. But the incorporation of strong compressive nitride liner film will reduce the drive current 2% comparing SCS to MCS conditions. The PMOS drive current was improved 5% by adopting strong compressive LDD spacer film with SCN condition. For different LDD spacers and stresses, very high saturation drive currents of Idsn = 1.02mA/um and Idsp = 470uA/um measured at 1.2V and an Ioff = 100nA/um can be achieved. A standard cell ring oscillator (RO) was used to evaluate AC performance of the different process combinations. Figure 4 shows that static ring oscillator leakage versus frequency was improved 4~5% by strong compressive LDD spacer film.

A manufacturing repeatable technique for improving transistor performance through LDD spacer strain engineering is demonstrated. For the first time, device performance improvements through elaborate optimization of LDD spacer film stress is combined with the traditional contact liner stress management. This scheme is embedded into a leading edge logic technology with 60nm gate length and nine layers of Cu metal interconnect. Drive current enhancement and ring-oscillator speed improvement are

observed by applying strong compressive spacer film. A microprocessor product of clock speed at ~1.5GHz@1.2V and overdrive to ~1.9GHz@1.5V as shown in fig.5 has been successfully fabricated with this process.

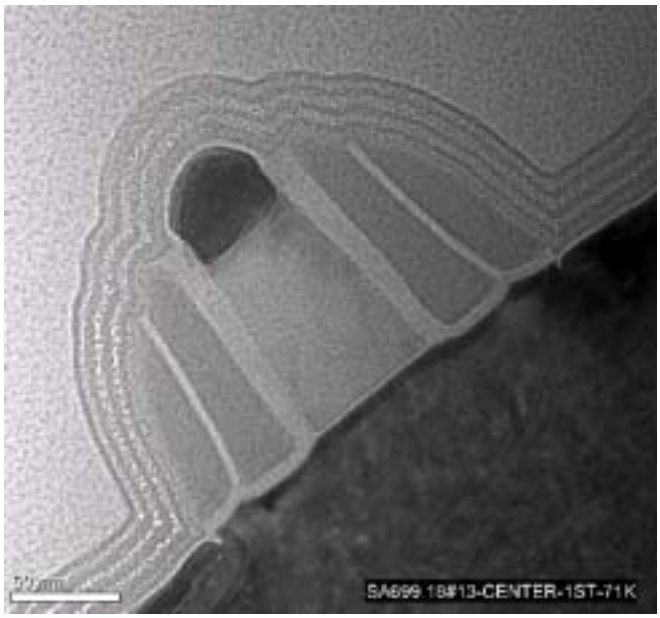

Fig.1 The TEM cross-section of 60nm gate length MOSFET with $CoSi_2$ on poly and source/drain.

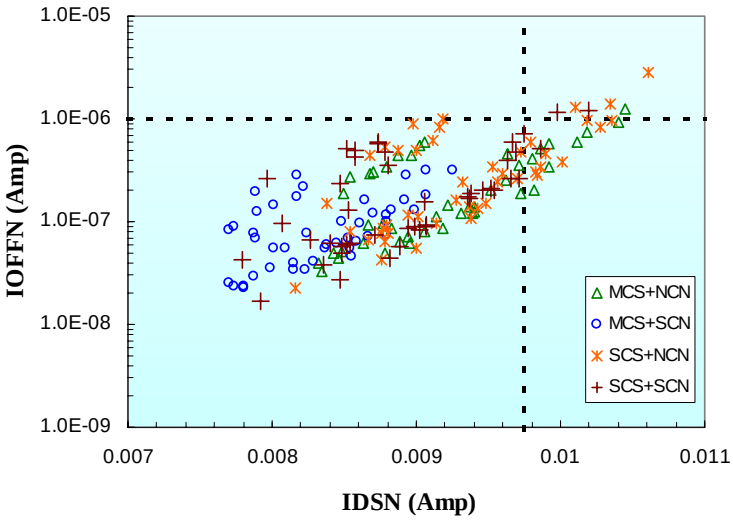

Fig.2 The drive current versus off-state leakage current characteristics of NMOS (W=10um) measured at 1.2V with different stress options of spacer and nitride etch stop films.

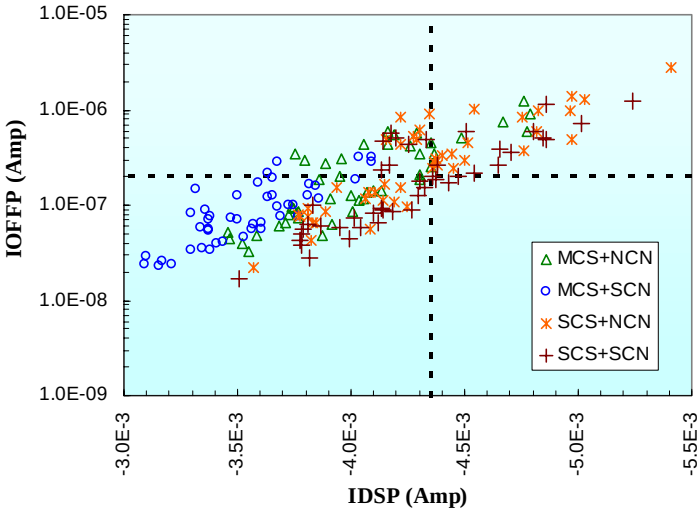

Fig.3 The drive current versus off-state leakage current characteristics of PMOS (W=10um) measured at 1.2V with different stress options of spacer and nitride etch stop films.

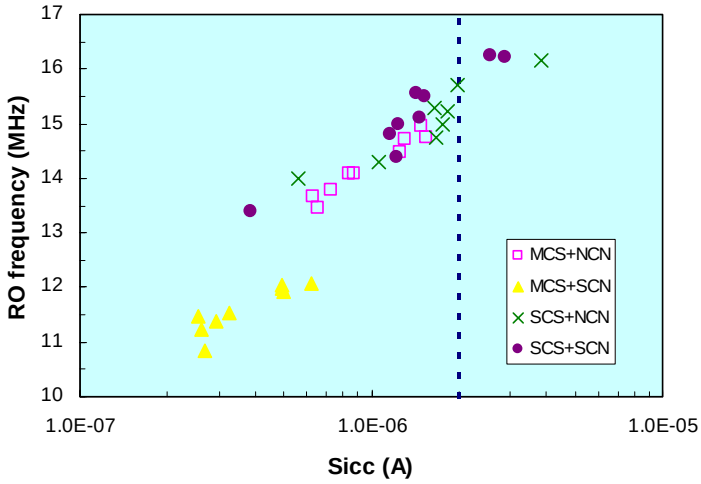

Fig. 4 The ring oscillator RO frequency versus static RO leakage characteristics measured at 1.2V. RO speed was improved 4~5% by strong compressive LDD spacer film.

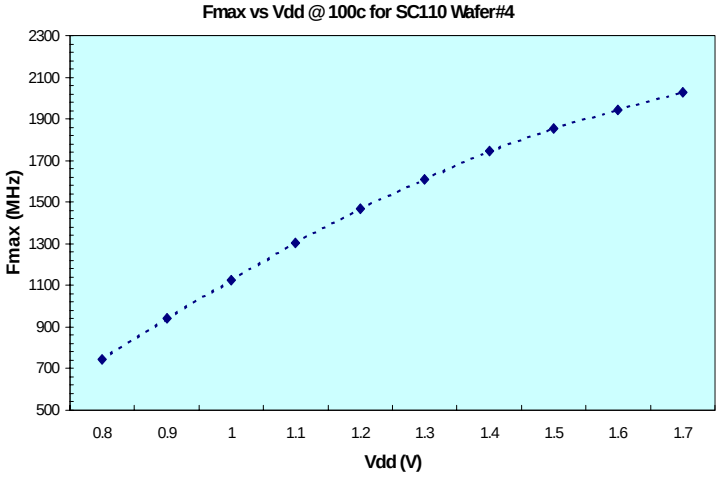

Fig.5 Characteristics of product speed versus Vdd.