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A Novel Simplified Process for Self Aligned Planar Wrapping Gate FET's with Directionally Crystallized Si Channel Processed via Sequential Lateral Solidification

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1. Introduction

Double gate [1] and wrapping gate [2] transistors are currently considered the most promising candidates for scaling CMOS down to sub – 100 nm regime because of their ideal subthreshold swing, excellent short channel immunity, and high current drivability. Process complexity, however, has been a serious technological barrier [3, 4]. Devices having simpler fabrication process reported in the past have low electron mobilities, severe channel thickness variations, and difficulties in achieving narrow width devices [5, 6].

In this work, we propose a novel simplified process for fully self aligned planar wrapping gate SOI FET structure with directionally crystallized ultrathin and highly uniform silicon channel. The directionally crystallized silicon channel in this new simplified process is formed from sequential lateral solidification with XeCl excimer laser and has good mobility and crystalline quality [7, 8, 9]. The directionally recrystallized silicon channel allows the intricacy of the fabrication process to become much simpler, along with the formation of ultrathin and highly uniform channel controlled only by LPCVD deposition. The mobility of the device is nearly same as that of SOI / bulk Si devices.

2. Fabrication Process

The 3 – D structure of the novel wrapping gate FET's at the gate poly deposition step is shown in Fig. 1. The wrapping gate is fully self aligned to the polysilicon source/drain and the channel is recrystallized Si. Fig. 2 shows the process flow of this self aligned planar wrapping gate SOI FET. LPCVD nitride and PECVD oxide deposited on Si substrate serve as the buffer layer during the recrystallization process as well as the blocking/sacrificial layer for device fabrication [Fig. 2 (a)]. Amorphous Si for the channel is deposited by LPCVD. The deposition rate of LPCVD with SiH_4 at 525 ºC is 10 Å / min. Ultrathin and highly uniform amorphous Si deposition is achieved with uniformity of 100 ± 2 Å and 400 ± 7 Å respectively across wafer for 100 Å and 400 Å thick films. As a result, the threshold voltage variation from the difference in the silicon thickness variation is much less than the devices with channel Si thickness, patterned by photolithography and etching.

Sequential lateral solidification of the a-Si film is conducted using a system that consists of 1) a 308 nm XeCl excimer laser, 2) a reticule mask with chevron-shaped apertures, 3) projection optics, and 4) a high-precision translation system. [10] (Lambada Physik LPX 315i, 308 nm XeCl). During this process, each pulse melted a linear region of ~ 2 µm wide and several cm long. The pulse is then translated by ~ 0.5 µm relative to the previous pulse in the direction perpendicular to the line of the beam.

Fig. 3 and Fig. 4 show the SEM and AFM of the recrystallized films by sequential lateral solidification of a 400 Å amorphous silicon on 3000 Å SiO_2 / 7000 Å Si_3N_4 / Si substrate after SECO etch. The orientation of the channel is arranged so that direction of current flow is parallel to the elongated grains and grain boundaries. Following the formation of the channel silicon, a CMP stopper layer consists of 4000 Å of LPCVD nitride is deposited, and the bar and holes for channel and source/drain are patterned by E – beam lithography and plasma dry etching [Fig. 2 (c)]. The source/drain region consisting of 1 µm n - doped polysilicon is deposited and patterned by CMP process with nitride stopping layer [Fig. 2 (d)]. Fig. 5 shows the SEM picture after polysilicon CMP. The sheet resistance of the doped poly silicon (doping concentration of 10^{20} cm^{-3}) is about 7 ohm / square after a minimum RTA annealing condition of 5 second at 1000 ºC.

After striping the nitride with H_3PO_4, source/drain isolation is achieved by removing the dummy polysilicon which is needed for minimizing the dishing effect during CMP of the polysilicon gate between source/drain regions using plasma dry etching. Silicon is also removed except in channel region during the same step to allow a path for the bottom gate [Fig. 2 (e)]. Fig. 6 shows SEM picture after stripping the nitride with H_3PO_4. Fig. 7 shows SEM picture after isolation, removal of recrystallized Si except in channel region, and removal of the bottom oxide for the realization of bottom gate with BOE. Gate poly is patterned using a CMP process after gate oxidation (45 Å) and doped polysilicon gate deposition (5000 Å). Top and bottom gate are fully self aligned to the polysilicon source/drain during this CMP process [Fig. 2 (f)].

3. Device Characterization

Fig. 8 shows the measured I–V characteristics for a device consisted of 2 µm channel width and 0.3 µm channel length. For this device, the channel doping is achieved by ion-implantation with 3.6E12/cm^2 Boron at 5 KeV, resulting in a Vth of about 0.5 V ~ 0.6 V. Drain current begins to saturate around V_d = 0.5 V and V_g = 1V. For $V_g – V_t$ = 0.5 V or 0.4 V and V_d = 0.5V, I_d is 500 µA / 2 µm. The large resistance between channel Si and source/drain regions arises from insufficient pre cleaning prior to the doped source/drain polysilicon which in turn causes the lower current. More developed pre cleaning can lower the parasitic resistance thereby increasing the drain current.

The residual stringers between the source and the drain during the dummy pattern etching results in the off current of $1X10^{-4}$ A. Fig. 8 (b) also shows the Id – Vg characteristics for a device with 2 µm channel width and 0.3 µm channel length with channel doping of $3.6X10^{12}cm^{-3}$ at V_d = 0.3 V. The subthreshold swing is 8 mV / decade. This low subthreshold swing is because of tunnelling through the native oxides between the channel poly and source/drain since floating body effect at V_d = 0.3 V is small.

4. Conclusion

A novel simplified process for fully self aligned planar wrapping gate SOI FET with directionally crystallized ultrathin and highly uniform Si channel is proposed and demonstrated for the first time. The transistor is based on the directionally crystallized silicon channel along the current flow direction whose mobility is nearly the same as that of SOI / bulk devices. Using directionally recrystallized silicon channel reduces the complexity of the fabrication process. Ultrathin and highly uniform silicon channel 100 ± 2 Å, controlled by LPCVD, is achieved.

5. Acknowledgements

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6. References

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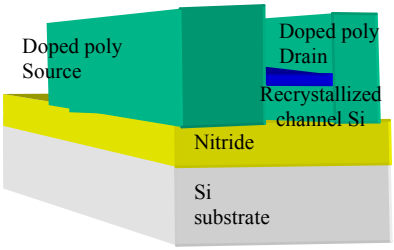
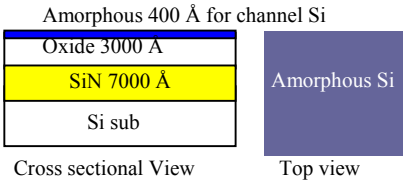
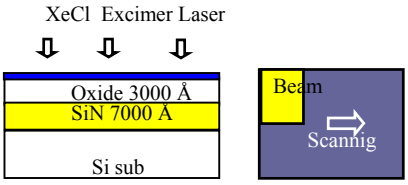


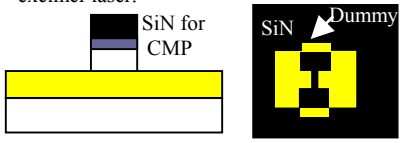
Fig. 1. The novel fully self aligned planar wrapping gate SOI FET with directionally crystallized ultrathin and highly uniformrm Si channel at the gate poly deposition step.



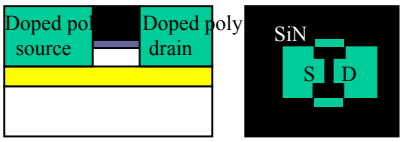
(a) Formation of ultrathin and highly uniform channel Si.



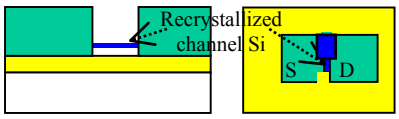
(b) Directional recrystallization by XeCl excimer laser.



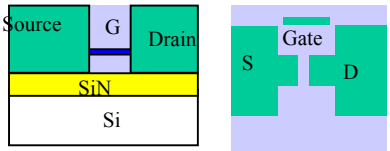
(c) Formation of bar and hole for the channel and source / drain using E – beam lithography. The layer between source / drain is dummy layer to minimize the dishing effect during gate poly CMP.



(d) Doped poly deposition for source / drain and CMP.



(e) Strip of channel SiN, isolation of source / drain, removal of channel Si except channel region, and removal of the bottom oxide for the path of bottom gate.



(f) Gate oxidation, gate poly deposition for top gate and bottom gate, and poly CMP for gate patterning.

Fig. 2. Process sequence of the proposed novel fully self aligned planar wrapping gate SOI FET with directionally crystallized untrathin and highly uniform Si channel.

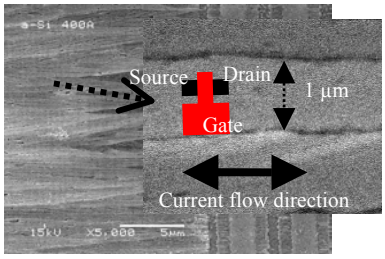


Fig. 3. SEM pictures of typical micro – structures obtained from directional crystallization method for amorphous Si 400 Å on oxide 3000 Å / nitride 7000Å / Si substrate after SECO etch.

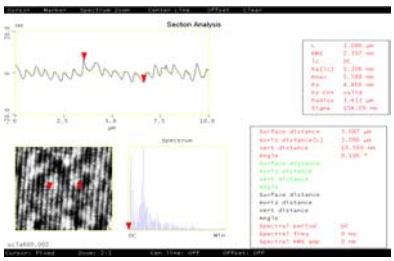


Fig. 4 AFM data of directional crystallization silicon for amorphous silicon 400Å after SECO etch

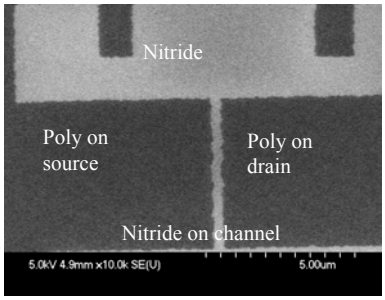


Fig. 5. SEM picture after poly CMP for channel width 5 μm and channel length 0.2 μm.

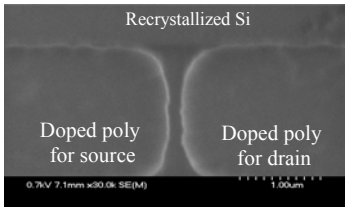


Fig. 6. SEM picture after stripping channel nitride for channel width 2 μm and channel length 0.3 μm.

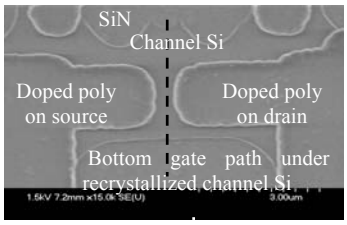
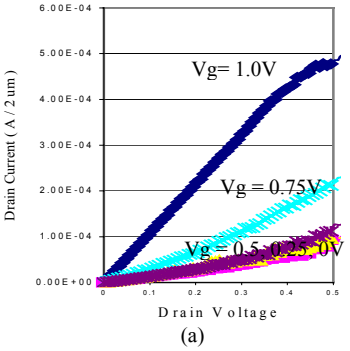
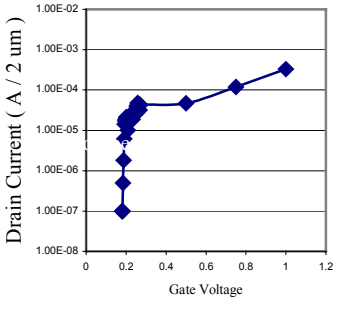


Fig. 7. SEM picture for width 2 μm and length 0.3 μm after isolation of source/drain, removal of recrystallized channel Si except in channel region, and removal of the bottom oxide for the realization of bottom gate.



(a)



(b)

Fig. 8. (a) Id – Vd curves for W= 2 μm and Lg = 0.3 μm with B 5keV 3.6E12 channel implantation and 400 Å channel thickness. (b) Id – Vg curve at Vd = 0.3 V for the same device.