Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.580-581

P3-2

Characterization of Embedded Poly-Heater PMOSFETs and its Application on In-Line Wafer Level NBTI Monitor

C. S. Wang[1, 2], W. C. Chang[1], W. S. Ke[1], C. T. Chiang[1], C. F. Lee[1], K. C. Su[1] and M. J. Chen[2]

[1]Quality and Reliability Assurance Div., United Microelectronics Corp.
[1]No3. Li-Hsin Rd. II, Science-Based Industrial Park, Hsinchu300, Taiwan
Phone: 886-3-5789158 E-mail: chi_shiun_wang@umc.com
[2]Department of Electronics Engineering, National Chiao Tung University
[2]1001 University Road, Hsinchu300, Taiwan

1. Introduction

Negative bias temperature instability in PMOSFETs has become the major reliability concern in state-of-the-art technologies [1]. However, seldom reliability control monitor concept is addressed before by the lack of "industry standard" procedure. Thus, it is necessary and urgent for us to come out an applicable concept and novel teststructure for NBTI reliability control monitor because a thorough reliability assurance usually consists of qualification phase and reliability control monitor phase.

For the first time, we propose a new and simple junction temperature extraction technique for embedded poly-heater PMOSFETs, and conduct it on in-line fast wafer level NBTI monitor.

2. Experimental Setup and Procedure

A stand-alone PMOSFET was embedded with a poly heater as shown in Fig. 1. The serpentine metal one layer above poly heater was used being the thermal sensor. PMOSFETs with extremely low aspect ratio, i.e. narrow width and long channel, were designed because it's the most critical geometry of NBTI performance, as shown in Fig. 2. This teststructure was fabricated by the standard 90nm CMOS process and without any extra treatment.

The negative bias temperature instability (NBTI) test procedures of this self-heating teststructure i) ramping up voltage on the poly heater, ii) calculating metal one temperature by the aid of temperature coefficient of resistance, and finally stop on target NBTI stress temperature, and iii) forcing a NBTI stress voltage on the gate terminal with source, drain, and bulk tightened to ground unit. Fig. 3 shows that metal temperature of 250°C can be reached around 3 sec.

3. Results and Discussion

Fig. 4 (a) and Fig.4 (b) show that there are no electrical performance difference between the conventional PMOSFET and this embedded poly-heater PMOSFET. The plasma-induced damage can be also avoided in this teststructure because of the poly-heater departure from the poly gate electrode. The plasma-induced damage immunity of this embedded poly-heater PMOSFET structure was examined by using conventional thermal-chuck NBTI test. Result was depicted in Fig. 5.

The NBTI stress temperature, i.e. junction temperature, was extracted from the series resistance of drain side, source side, and the inversion channel. Some literature [2] uses the I-V curve of p/n (drain/bulk) junction to calculate junction temperature, however, the ideality factor and I-V exponential relationship will significantly affect the temperature validity.

Here, for the first time, we use the linearity relationship between temperature and the series resistance as shown in Fig. 6 and Fig. 7. The PMOSFET was biased under linear region such that the inversion resistance was formed. Conjugating with existence drain and source resistance will lead to PMOSFET turn-on resistance. And the turn-on resistance will vary with the ambient temperature by the formula

$$R(T) = R_{REF} \times \left[1 + TCR \times \left(T - T_{REF}\right)\right] \quad (1)$$

where R_{REF} is resistance under reference temperature. Finally, the temperature correlation between metal temperature and junction temperature can be deduced, shown in Fig. 8. The correlation result was verified by checking NBTI degradation in thermal-chuck as well as embedded poly-heater. Consistent result is shown in Fig. 9.

We utilize this fast self-heating teststructure to be the candidate of in-line NBTI monitor. According to [3], the suitable stress voltage of NBTI monitor can be determined from the charge separation technique to prevent from TDDB stress regime as shown in Fig. 10. It is worthy to address that the measured terminal currents of our long channel device (L=10um) through this work are significantly different from those of short channel device (shown in [3]). The main root cause can be attributed to the too long distance for those generated holes via gate emission impact ionization to flow back into source/drain regions. Therefore, source/drain currents reversal phenomenon can only be observed in short channel devices.

Both the stress duration and monitor spec can be determined by applying voltage scaling and degradation scaling. A NBTI monitor of this self-heating PMOSFET is shown in Fig. 11.

4. Conclusions

We have proposed a new and simple technique to extract the junction temperature of the embedded poly-heater PMOSFETs, and its application on real case in-line NBTI monitor for 90nm CMOS technology has been also successfully demonstrated. Therefore, we have provided a thorough and applicable concept on NBTI in-line monitor.

Acknowledgement

The authors would like to express their honest acknowledgement to Rita Chen and C. M. Teng for their kind help during the work.

References

[1] G. La Rosa et al., in *proc., IRPS.*, pp.282-286, 1997.
[2] W. Muth et al., in *proc.,ICMTS.*, pp.155-160, 2003.
[3] C. S. Wang et al., in *proc., IPFA.*, pp.315-318, 2004.

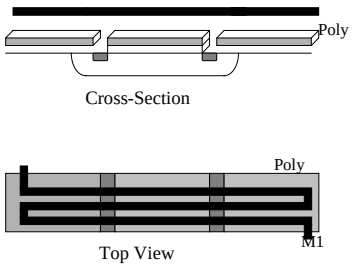


Fig. 1 Cross section view and top view of embedded poly-heater PMOSFET.

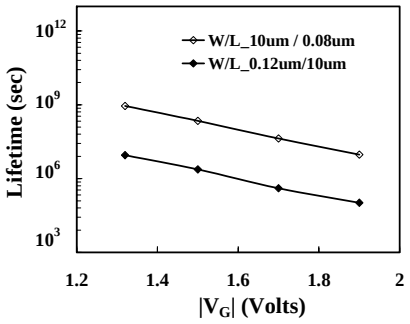


Fig. 2 Geometry dependence evaluation on NBTI.

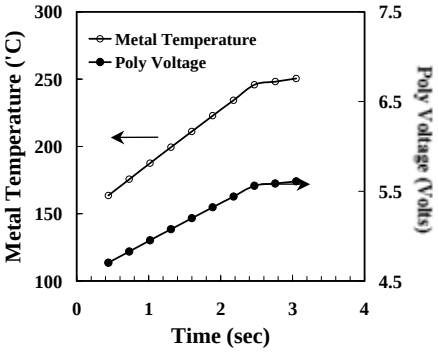
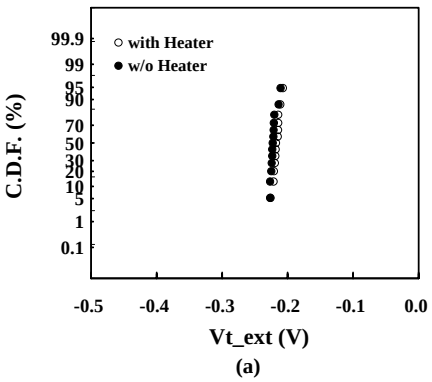


Fig. 3 Calculated metal temperature and measured poly voltage during ramp up procedure.



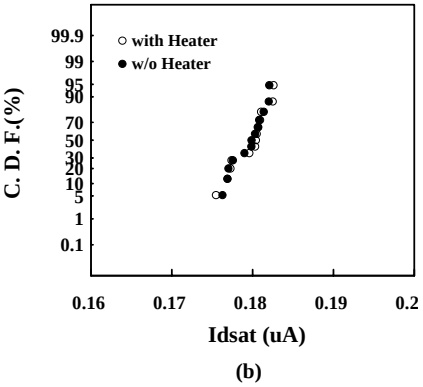


Fig. 4 Measured (a) threshold voltages, and (b) saturation currents of PMOSFETS with and without poly-heater.

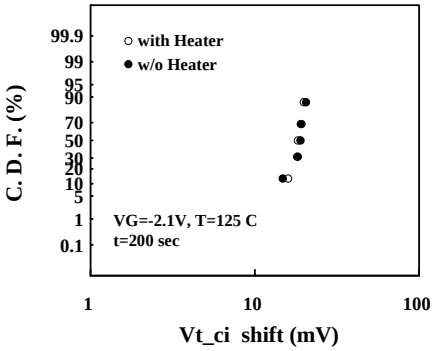


Fig. 5 Conventional NBTI test on PMOS-FETs with and without poly-heater.

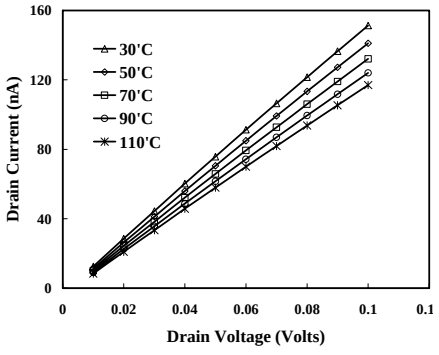


Fig. 6 Measured drain terminal currents under different ambient temperatures.

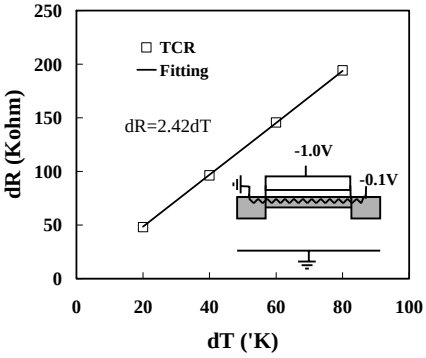


Fig. 7 Calculated turn-on resistances under different ambient temperatures.

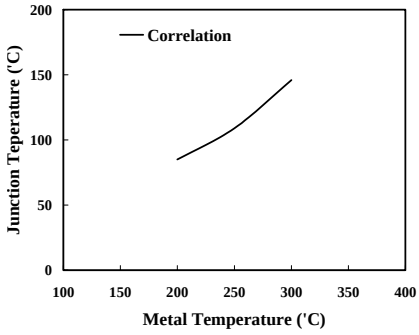


Fig. 8 Correlation plot of junction temperature and metal temperature.

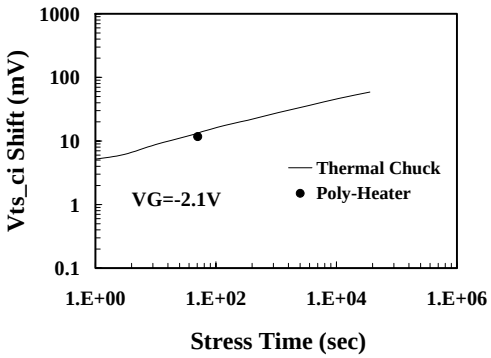


Fig. 9 Consistency check of NBTI degradation by using chuck and embedded-poly heater.

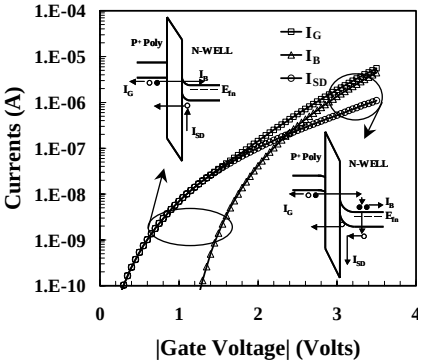


Fig. 10 Measured terminal currents of charge separate bias configuration. The energy band diagrams depict NBTI and TDDB regimes respectively.

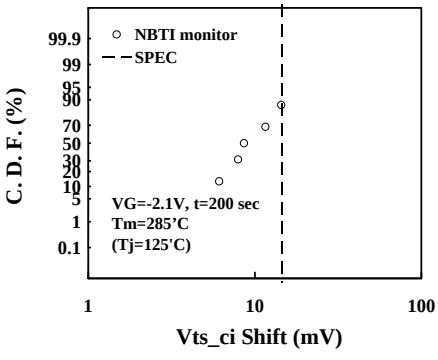


Fig. 11 A real case in-line NBTI monitor on 90nm CMOS technology.