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The Characteristics and Reliability of Multi-channel Poly-Si TFTs

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1. Introduction

The Polysilicon thin-film transistors (poly-Si TFTs) with narrow channel width were reported to have better performance such as lower threshold voltage and smaller subthreshold swing due to grain boundary trap states reduction. It has been reported that the existence of regions in the channel near the pattern edge where the grain boundary trap state density is much lower than elsewhere in the poly-Si channel [1][2]. Moreover, some reports have demonstrated that the gate electrode layer across the channel may induce side-channels in both sides of the channel region and these side-channels will increase the effective channel width. It was revealed that average carrier concentration in the channel region of the poly-Si gate electrode corner is increased by the electrostatic focusing from the top gate and both side gates of the stripes [3]. It is believed that the gate control capability is improved obviously due to narrow channel width. Accordingly, poly-Si TFTs with narrow and multiple channels have been proposed to enhance the electrical characteristics [3-6]. However, there was almost not complete reliability analysis of poly-Si TFTs with multiple channels.

In this study, we first demonstrate that the fabrication process and electrical characteristics of n-channel ploy-Si TFTs with different stripes. We can see that poly-Si TFTs with multiple channels have better performance than the conventional TFTs. Then, we investigated the reliability issue of poly-Si TFTs with multiple channels.

2. Experimental

Fig. 1 shows the process flow of the proposed poly-Si TFT. First, 500-nm-thick thermal oxide was grown on the Si wafers for the glass substrate. Then, 100-nm-thick amorphous silicon layers were deposited and recrystallized. A 50-nm-thick TEOS oxide was deposited for gate insulator. Then, the poly-Si film was patterned and etched to be the gate electrode. The regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15} ions/cm^{-2} at 40 keV, respectively. Finally, a passivation layer was deposited and patterned to complete contact metallization, devices were passivated by NH_3 plasma treatment for 2 hours at 300 ℃.

3. Results and Discussion

The schematic cross-sectional diagram of the structure is shown in Fig. 2. The transfer characteristics of the conventional and proposed TFTs of the effective channel width is 40 μm with single, 4, 8, 20, and 40 stripes, respectively (Fig. 3). The detail data of these structures were summarized in Table I. In the 40 stripes channel, it shows better electrical performance on threshold voltage reduction, higher mobility and ON/OFF ratio, and better subthreshold swing. Figure 4 illustrates the output characteristics of the conventional and the proposed poly-Si TFTs with different stripes of channel. ($V_G - V_{th}$ = 0.5; 2; 3.5 V). By normalized the gate voltage, the multi-channel device shows the better kink effect immunity due to superior gate control ability. Figure 5 shows the on-state current and field effect mobility versus the number of channel stripe form 1 to 40.

Moreover, we will also discuss the reliability issue of the conventional and proposed TFTs that the effective channel width is 20 μm with single, 2, 4, 10, and 20 stripes, respectively, shown in Fig. 6 and 7. When HCS was applied to the TFT, numerous electrons were injected into the gate oxide and captured by the traps, resulting in the degradation of I_{ON}. The distribution of V_{th} for different channel width in TFTs with different channel stripes were shown in Fig. 7. The TFTs with channel stripes of 40 show more degradation on V_{th} distribution than those with one stripe channel. This could be due to the drain side electrical field enhancement effect on the multi-channel TFTs. The devices with numbers of channel stripes show more serious instability issue in device characteristics.

3. Conclusions

The effects of multi-channel TFTs on the performance and reliability have been investigated. As the channel stripes increased, the initial characteristics show better performance. However, the reliability becomes more severe. Therefore, for the fabrication of high reliable devices and yield improvement, the multi-channel structures must be carefully designed.

Acknowledgements

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References

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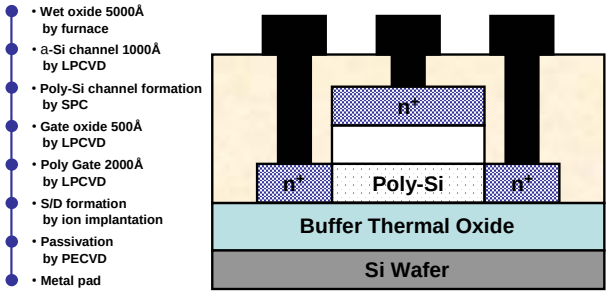

Fig. 1 Process flow of the conventional and multi-channel poly-Si TFTs.

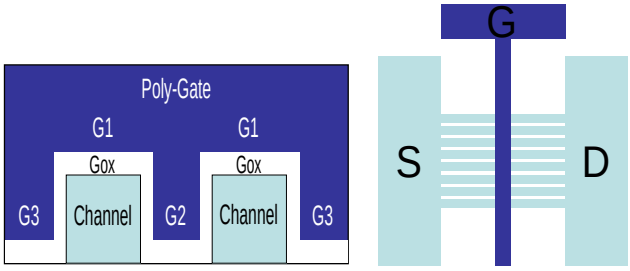

Fig. 2 Cross-section of the multi-channel poly-Si TFTs parallel and perpendicular to the direction of the source and drain electrode.

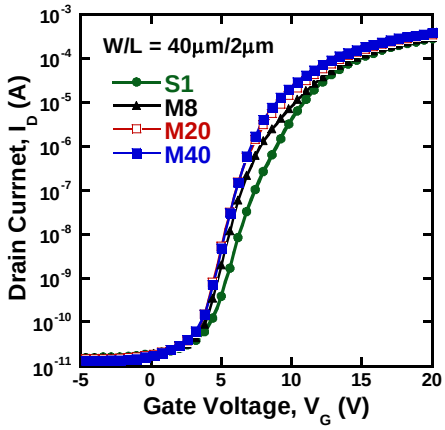

Fig. 3 Transfer characteristics of the conventional and proposed poly-Si TFTs with different stripes of channel.

Table I Device characteristics of the multi-channel TFTs.

	S1	M4	M8	M20	M40
V_{th}(V)	9.43	9.08	8.39	7.66	7.51
S.S(V/dec.)	1.257	1.270	1.230	0.987	0.923
μ_{eff} (cm²/V.s)	25.3	25.7	26.1	28.5	29.6
I_{on} @ V_G = 20V(A)	2.76×10^{-4}	2.78×10^{-4}	2.96×10^{-4}	3.44×10^{-4}	3.76×10^{-4}
I_{off} @ V_G = -5V(A)	1.56×10^{-11}	2.06×10^{-11}	1.56×10^{-11}	1.51×10^{-11}	1.43×10^{-11}
ON/OFF Ratio	1.79×10^{7}	1.61×10^{7}	1.91×10^{7}	2.37×10^{7}	2.89×10^{7}
N_t(cm⁻²)	5.80×10^{12}	5.84×10^{12}	5.71×10^{12}	5.40×10^{12}	5.06×10^{12}

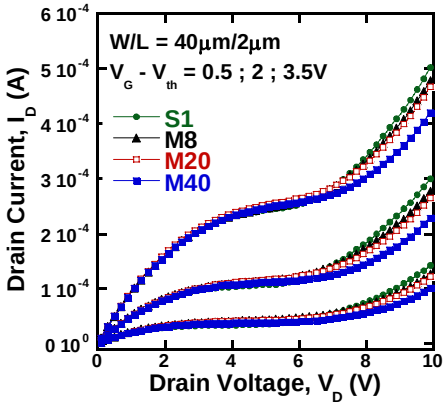

Fig. 4 Output characteristics of the conventional and the proposed poly-Si TFTs with different stripes of channel. ($V_G - V_{th}$ = 0.5; 2; 3.5 V).

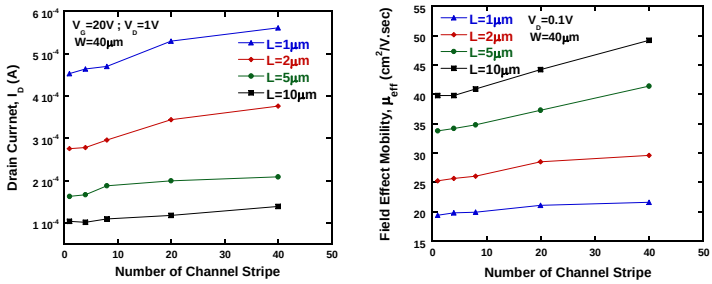

Fig. 5 (a) On-state current and (b) field effect mobility as a function of the number of channel stripes.

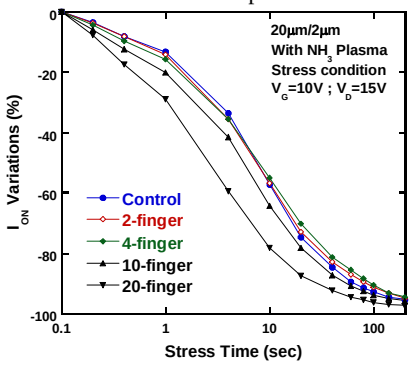

Fig. 6 On current variation in different stress time in V_G=10 V and V_D=15 V for 200 s.

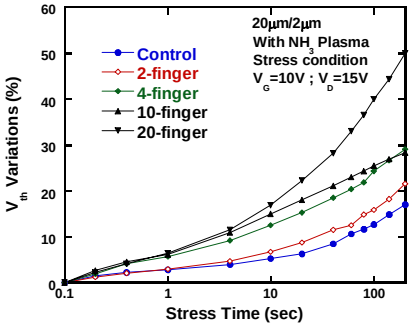

Fig. 7 Threshold voltages with different channel fingers under stress conditions.