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Effective Prevention of Single Event Burnout for N-Channel Power MOSFETs

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Abstract

This paper presents prevention technologies of single-event burnout (SEB) for power metal-oxide-semiconductor field-effect transistors (MOSFETs) in a space environment. The power MOSFET structures are investigated to simultaneously prevent the SEB and maintain normal characteristics. The optimal device structure has been developed to exhibit the best immunity against the SEB.

1. Introduction

Power metal-oxide-semiconductor field-effect transistors (MOSFETs) with high switching speed characteristics have been widely used for space applications [1]. In a space environment, power MOSFETs and integrated circuits, however, are susceptible to single-event burnout (SEB) due to heavy ions passing through power MOSFETs biased in the OFF state [2]. Electron-hole pairs are generated along the ion track and transient currents initially turn on the parasitic bipolar junction transistors (BJTs) in power MOSFETs. Permanent damage results from the SEB. In this paper, we comprehensively study how power MOSFET structures influence the device immunity against the SEB.

2. Device Structures

Five different structures of n-channel power double-diffused metal-oxide-semiconductor (DMOS) are investigated. The conventional n-channel power DMOS transistor (structure A) is shown in Fig. 1(a). The power MOSFET with an additional p^+-plug (structure B) is illustrated in Fig. 1(b). The power MOSFET with lateral extension of the p^+ plug (structure C) and that with both the lateral and vertical extensions of the p^+ plug (structure D) are shown in Figs. 1(c) and 1(d), respectively. Fig. 1(e) shows that the p^+ plug of the power MOSFET (structure E) has the same lateral extension length as those of the structure-C and structure-D devices. Moreover, the p^+-plug and p-base regions of the structure-E power MOSFET have the same depth.

3. Results and Discussion

The SEB and normal operation characteristics of the power MOSFETs are studied by a two-dimensional numerical simulator, Medici. Fig. 2 shows the breakdown characteristics of the power MOSFETs with structures A, B, C, D, and E. It is seen that the power MOSFET with the structure E has almost the same breakdown voltage as that with the structure A. Fig. 3 shows the current flow lines in the structure-E power MOSFET due to triggering of heavy ions. The ion impact position is at X = 2 μm. When the structure-E power MOSFET biased in the OFF state (Both the gate voltage (V_G) and source voltage (V_S) are 0 V) is hit by a Br ion with an energy of 180 MeV according to linear energy transfer (LET) theory, at an impact position of X = 2 μm. The drain current (I_D) characteristics of the structure-E device for different drain voltage (V_D) values, 210 V and 220 V, are shown in Fig. 4. It can be clearly seen that the structure-E power MOSFET is liable to burnout at V_D = 220 V while it is safe from SEB at V_D = 210 V. Fig. 5 shows the drain current characteristics of the structure-E power MOSFET as a function of ion impact positions. The device is biased at V_G = 0 V, V_S = 0 V, and V_D = 190 V. The energy of the incident Br ion (E_{Br}) is 180 MeV. Five different ion impact positions, X = 2 μm, 4 μm, 6 μm, 8 μm, and 10 μm, are investigated. The results show that the device is susceptible to the SEB at the X positions of 8 μm and 10 μm. In order to investigate how the device structures influence the power MOSFETs in terms of the SEB, comprehensive research is conducted. Table I lists a SEB occurrence summary for power MOSFETs hit by a Br ion with an energy of 180 MeV. The ion impact position is at X = 2 μm. The structure-E power MOSFETs are not affected by the SEB before the V_D is higher than 210 V.

4. Conclusions

The n-channel power MOSFETs with five different structures have been studied in order to have good immunity against the SEB. The structure-E power MOSFETs with the lateral extension of the p^+ plug as well as the equal depth of the p^+-plug and p-base regions demonstrate excellent capability to prevent the SEB for space applications.

Acknowledgements

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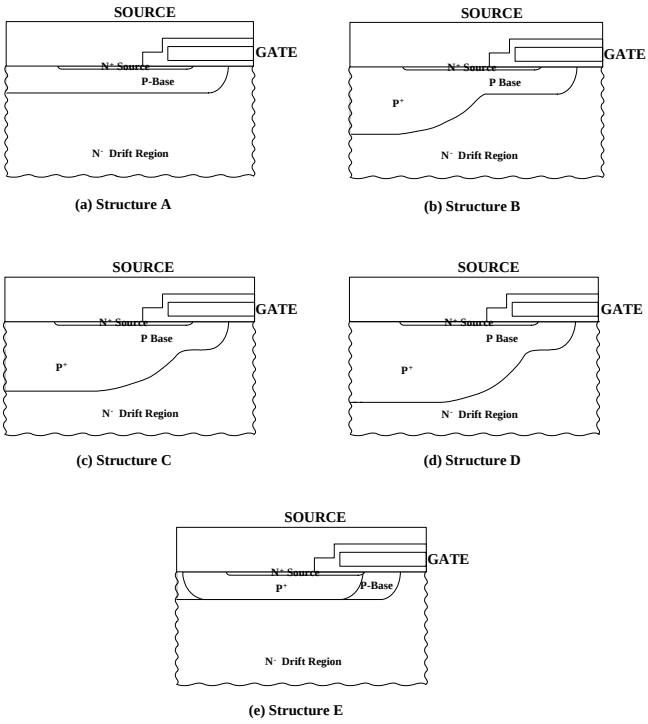

Fig. 1. Cross sectional views of n-channel power MOSFETs. (a) Structure A. (b) Structure B. (c) Structure C. (d) Structure D. (e) Structure E.

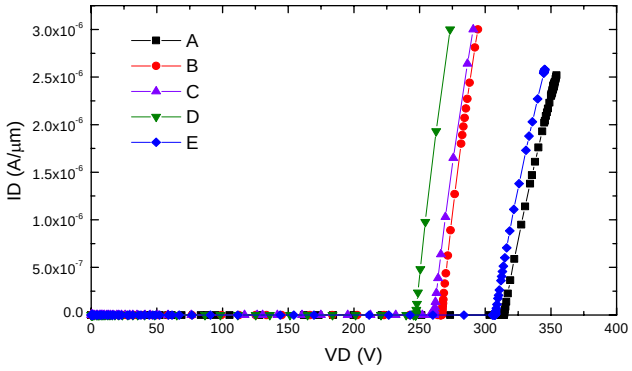

Fig. 2. Breakdown characteristics of the power MOSFETs with structures A, B, C, D, and E.

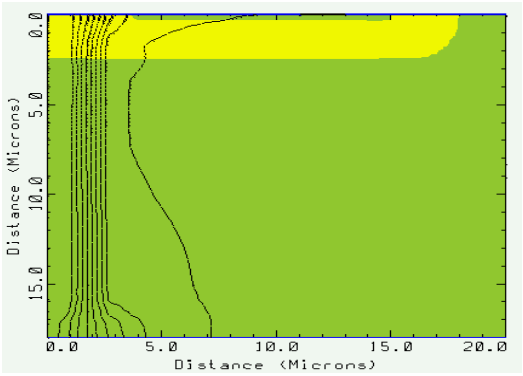

Fig. 3. Current flow lines in the structure-E MOSFET due to triggering of heavy ions. The ion impact position is at X = 2 μm.

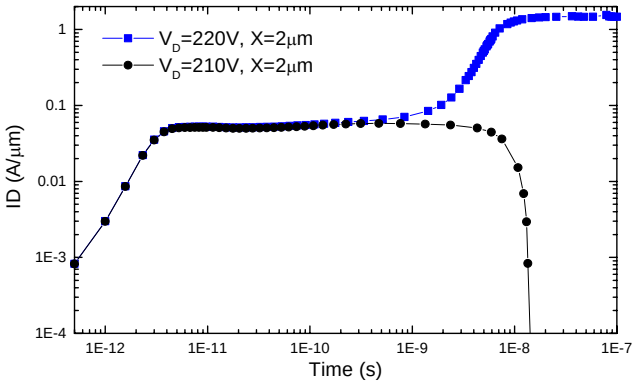

Fig. 4. Drain current (I_D) characteristics of the structure-E MOSFET.

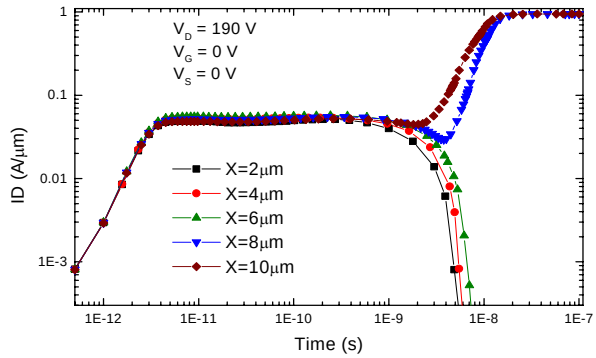

Fig. 5. Drain current characteristics of the structure-E power MOSFET as a function of ion impact positions. E_{Br} = 180 MeV.

TABLE I
SEB OCCURRENCE SUMMARY (E_{Br} = 180 MeV and X = 2 μm)

V_D (V) / Structure	10	30	50	70	90	110	130	150	170	190	210	230	250	270
A	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
B	No	No	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
C	No	No	No	No	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
D	No	No	No	No	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
E	No	No	No	No	No	No	No	No	No	No	No	Yes	Yes	Yes