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DC Hot Carrier Reliability at Elevated Temperatures for nMOSFETs Using 0.13μm Technology

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1. Introduction

It is well known that under certain bias conditions, hot carriers in MOS transistors will result in property degradation due to damage in the gate oxide and its interface states. As to the hot carriers on elevated temperature devices, the degradation of saturation drain current for high drain bias was said worse due to the reduction of velocity saturation length; however, the degradation of linear drain current was smaller with increasing stress temperature [1]. Other previous studies showed that the hot carrier effect existed a transition voltage (or called transition point), which reversed the dependence of MOSFETs' properties to temperature [2,3]. This finding was proved with the peak substrate current would reverse its temperature dependence when biased drain voltage V_d across the transition voltage and implied that more degradation at elevated temperature occurred only at low V_d. Another conflict findings reported that the degradation would more serious when stressed at $V_g = V_d$ and in high temperature, even the biased V_d already larger than the transition voltage [4].

In this report, we present the hot carrier degradation of $I_{d,op}$ (defined based on analog application) is the worst case, which is important for analog circuit design. In addition, the reverse temperature effect, which denotes the property degradation becomes worse in high temperature, was found in devices with L_{eff} = 90 nm but not in 120 nm.

2. Experiments and Results

Tested devices were from 0.13 μm technology. The nMOSFETs used in these experiments have L_{eff} = 120 nm with gate oxide thickness of 32 Å and L_{eff} = 90 nm with gate oxide thickness of 20 Å, all with W = 10 μm. Stress conditions were (1) 25 ℃ (2) 75 ℃ (3) 125 ℃, all at peak substrate current. The measurement conditions are as in the Table I .

For 90 nm devices, Fig. 1 shows the experimental $I_{d,sat}$ degradation versus stress time at different temperatures for stressed at V_d = 2.2 V. As expected in [1], the degradations are increased as temperature rose from 25 ℃ to 125 ℃ due to the reverse temperature effect.

Fig. 2 shows the degradation ratios of drain currents with different temperatures. Among them, degradation of $I_{d,op}$ at 125 ℃ is the worst case. For digital circuits, $I_{d,lin}$ is worse than $I_{d,sat}$.

For 120 nm devices, the stress bias was initially set higher than the transition voltage, which was reported at around 2.4 V. It is clear that Fig. 3 shows no reverse temperature effect. Degradation of drain current at room temperature is still more serious than the currents with higher temperatures. Fig. 4 shows the degradation ratios of drain currents versus different temperatures. The degradation of $I_{d,op}$ is still the largest in all temperature range, and $I_{d,lin}$ is worse than $I_{d,sat}$. Also note that the trends in Fig. 2 and Fig. 4 are quite different.

For the cases in Fig. 5, 6, and 7, the drain bias was intended to set lower than transition voltage. Unlike 90 nm devices, it is still no reverse temperature effect for three kinds of drain currents. In addition, the room temperature still possesses the highest degradation among different temperatures. Fig. 8 indicates same situation. The reverse temperature effect still can not be found even the drain bias has been lower than the reported transition voltage. In this stress condition, $I_{d,op}$ is still the worst case for analog applications and $I_{d,lin}$ is worse than $I_{d,sat}$.

3. Conclusions

This paper, for the first time, shows that, the hot carrier degradation of $I_{d,op}$, which is based on analog operation condition, is the worst case. This result should be a valuable message for analog circuit designers. As for the reverse temperature effect and the transition voltage, this study finds no consistent phenomena.

References

[1]. H. Hwang, et al., *IEEE International Reliability Physics Symposium 33rd Annual Proceedings.* (1995) 48.

[2]. P. Aminzadeh, et al., *Symposium on VLSI Technology, Digest of Technical Papers.* (1998) 178.

[3]. W. Wang, et al., *IEEE International Integrated Reliability Workshop, Final Report,* (1999) 66.

[4]. E. Li, et al., *IEEE International Reliability Physics Symposium, 38th Annual Proceedings.* (2000) 103.

Table I The measurement conditions unit: V

		L_{eff} = 90 nm		L_{eff} = 120 nm	
		V_g	V_d	V_g	V_d
Digital	$I_{d,lin}$	1.2	0.05	1.8	0.05
	$I_{d,sat}$	1.2	1.2	1.8	1.8
Analog	$I_{d,op}$	0.53	0.6	0.68	0.9

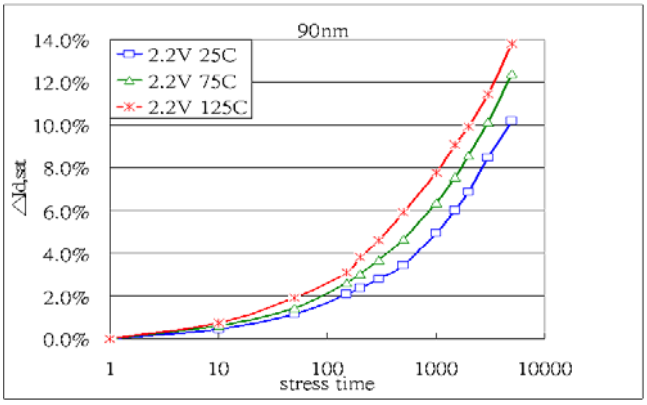

Fig. 1 $\triangle I_{d,sat}$ versus stress time at V_d = 2.2 V with different temperatures.

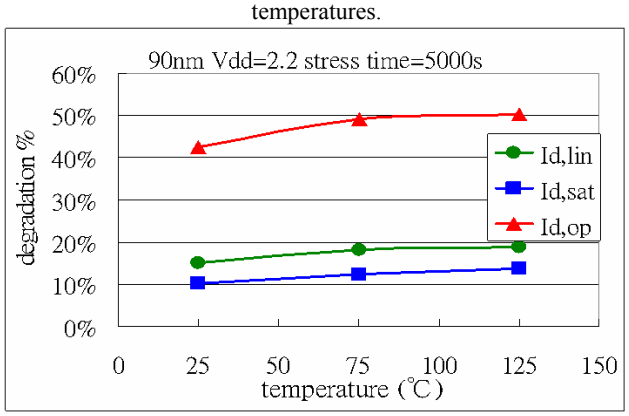

Fig. 2 Drain current degradation versus temperature at V_d = 2.2 V after stress 5000 seconds.

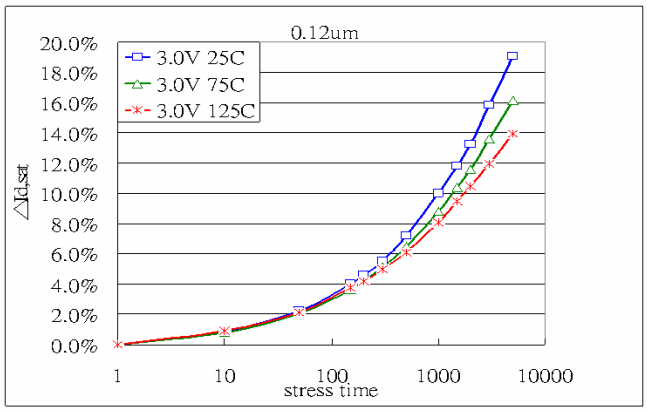

Fig. 3 $\triangle I_{d,sat}$ versus stress time at V_d = 3.0 V with different temperatures.

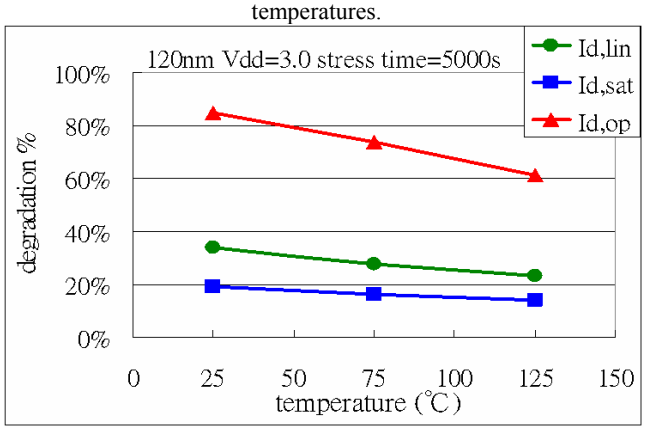

Fig. 4 Drain current versus temperature at V_d = 3.0 V after stress 5000 seconds.

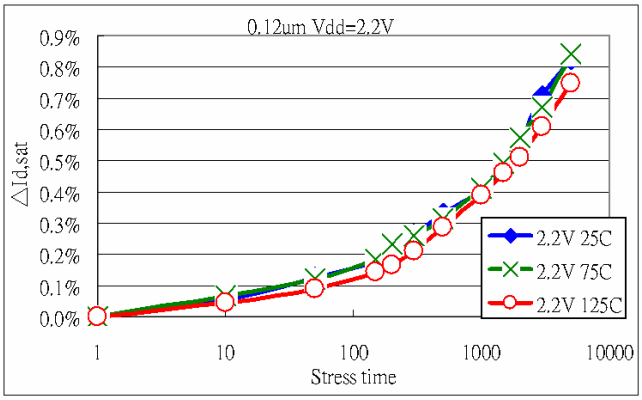

Fig. 5 $\triangle I_{d,sat}$ versus stress time at V_d = 2.2 V with different temperature.

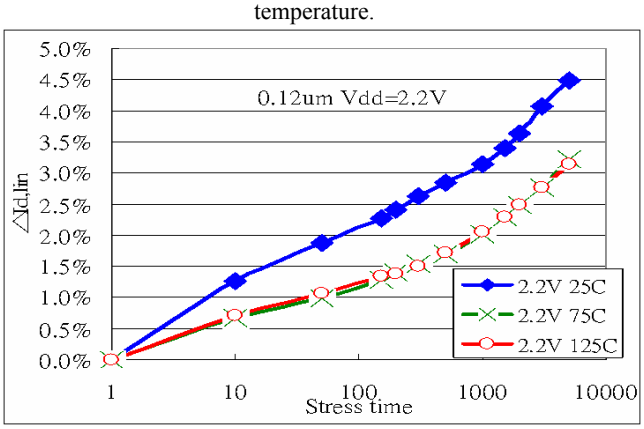

Fig. 6 $\triangle I_{d,lin}$ versus stress time at V_d = 2.2 V with different temperature.

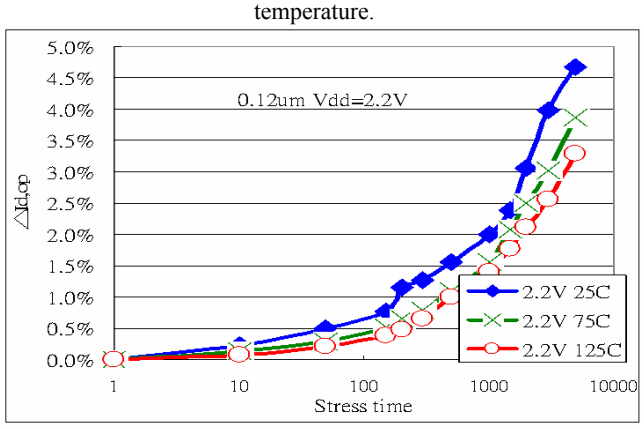

Fig. 7 $\triangle I_{d,op}$ versus stress time at V_d = 2.2 V with different temperature.

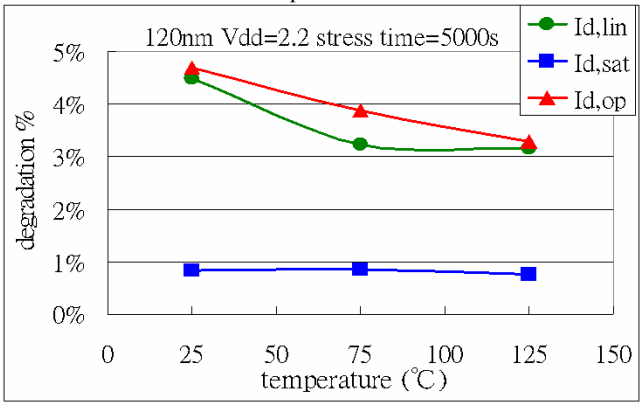

Fig. 8 Drain current degradation versus temperature at V_d = 2.2 V after stress 5000 seconds.