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Investigation of Accumulation-mode Vertical Double-gate MOSFET

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1. Introduction

Because of their intrinsic strength against the SCEs, DG-MOSFETs have been regarded as the most scalable CMOS devices [1]. However, as the device size is decreased by less than 10 nm, the S/D formation becomes a big concern even for the DG-MOSFET. Especially, fabrication of extremely abrupt p-n junctions and control of the overlap between the gate and S/D extension are very challenging for FET operating in the inversion mode. An alternative option is to operate such nm-scale FETs in the accumulation mode [2]. In this case, careful control of the overlap between the gate and S/D extension is no longer needed (**Fig. 1**). Furthermore, an accumulation-mode PMOS (n^+-DG on a p-channel) is very advantageous thanks to no boron penetration from the gate and minimized gate depletion. Nevertheless, little is known on fundamentals of the accumulation-mode DG-MOSFETs. In this paper, we investigate the accumulation-mode vertical DG-MOSFETs based on the experimental and simulation data.

2. Vertical DG-MOSFET Fabrication

The fabrication processes of the accumulation- and inversion-mode vertical DG-MOSFETs are summarized in **Fig. 2**. For both cases, vertical ultrathin channels (UTCs) were formed on p-type Si(110) wafers using orientation-dependent-wet etching (ODWE) [3]. The ODWE was performed in 2.38% TMAH at 50˚C. Thanks to slimming of both the EB resist and SiO_2 hard mask, a 20-nm-thick UTC was easily formed using the 80-nm-thick resist pattern as shown in **Fig. 3**. It is also obvious that the ODWE well contributes to the LER improvement. In the case of the accumulation mode, after stripping the SiO_2 masks, dopant ions were perpendicularly implanted onto the UTC. As a result, the UTC regions were totally doped with dopants. On the other hand, in the inversion mode case, the mask SiO_2 was left to protect the UTC from the doping. Doping for the top region was done by the P solid-phase-diffusion from PSG. The in-situ P-doped poly-Si was used for a DG material and an etched-back process by RIE was used to form DGs. After the TEOS-CVD SiO_2 deposition, self-aligned-contact (SAC) holes were opened by using the planarization by an EB resist application and the following etchback (**Fig. 4**). **Fig. 5** proves that a high aspect (T_{Si}/H_{Si}= 20/200 nm) UTC formed by the ODWE never snaps over 24 μm which corresponds to W_g. T_{ox} and L_g were 5 nm and 100 nm for the accumulation-mode FET while 3 nm and 160 nm for the inversion-mode FET. The channel dopant concentrations (N_{body}) for the accumulation- and inversion-mode were $5x10^{17}$ and $1x10^{16}$ cm^{-3}, respectively.

3. Results and Discussion

Fig. 6 shows I_d-V_g characteristics for the accumulation- and inversion-mode vertical NMOS DG-MOSFETs. In the long-L_g inversion-mode case, V_{th} hardly shifts and s-slope maintains low value with increasing T_{Si}. On the other hand, the short-L_g accumulation-mode DG-MOSFETs exhibit severe influence of T_{Si} on the V_{th} and s-slope. It is noteworthy, however, that by decreasing T_{Si}, both the V_{th} and s-slope are dramatically improved to the same values as those for the long-L_g inversion-mode DG-MOSFETs, as shown in **Fig. 7**. We then explore the impact of N_{body} on V_{th} and s-slope for the accumulation-mode DG-MOSFETs based on a device simulation. The relationship between V_{th}, T_{Si} and N_{body} is given by,

$$\pm\Delta V_{th} = qN_{body}T_{Si}/2C_{ox} . \quad \text{(- for n-type, + for p-type)} \quad -(1)$$

As shown in **Fig. 8**, when T_{Si} is thick, the difference between the simulated V_{th} and that estimated from Eq. (1) becomes larger and s-slope becomes worse for the accumulation-mode case with increasing N_{body} as compared with the inversion-mode case. This means that the SCEs are enhanced for the accumulation mode with increasing N_{body} and T_{Si}. However, if T_{Si} is decreased to 10 nm, V_{th} corresponds to that estimated Eq. (1), and s-slope maintains low value (60 mV/dec.) regardless of N_{body}. It is also clearly from **Fig. 9** that the trend of the SCE in the accumulation mode is almost the same as that in the inversion mode if T_{Si} is sufficiently thin. It is thus concluded that the SCEs are well suppressed even in the accumulation mode by decreasing T_{Si}. In addition, if T_{Si} is sufficiently thin, V_{th} can be tuned by controlling N_{body} without degradation in s-slope even in the accumulation mode. Then we experimentally demonstrate V_{th} tuning by controlling N_{body} for the accumulation-mode PMOS vertical DG-MOSFET. As predicted from Eq. (1), a very high N_{body} would be required to control V_{th} as T_{Si} is scaled down. For example, a doping concentration of N_{body} = $1x10^{18}$ cm^{-3} would shift V_{th} by only 93 mV for T_{Si} = 20 nm and T_{ox} = 2 nm. In the inversion mode, the practical limitation in N_{body} exists due to the band-to-band tunneling in p-n junctions [4]. Contrarily, since there are no p-n junctions in the channel in the accumulation mode, a high N_{body} can be used to control V_{th}. As shown in **Fig. 10**, in the low N_{body} case (simulation), V_{th} becomes significantly higher with the use of n^+-DGs. However, by using high N_{body} of $3x10^{18}$ cm^{-3} and n^+-DGs, an appropriate V_{th} as well as a low s-slope can be attained for the PMOS DG-MOSFET. Of course, precise nm-scale control of T_{Si} is demanded in this technology. Fortunately the ODWE is exceedingly helpful for the nm-scale T_{Si} controllability.

4. Summary

Based on the experimental and simulation data, it was found that the SCEs are well controlled even in the accumulation mode FET by decreasing T_{Si}. Thus the accumulation-mode DG-MOSFET is concluded to enjoy the superior advantage of DG device structure. Furthermore, the accumulation-mode DG-MOSFET can offer not only the wider process window of manufacture, but also the easier V_{th} tuning by means of the control of N_{body}.

References: [1] T. Sekigawa, et al., Solid-State Electron. 27(1984)827. [2] F.-L. Yang, et al., Symp. VLSI Tech. (2002)104. [3] M. Masahara, et al., IEDM (2002) 949. [4] M. Ono, et al., Symp. VLSI Tech. (1994)147.

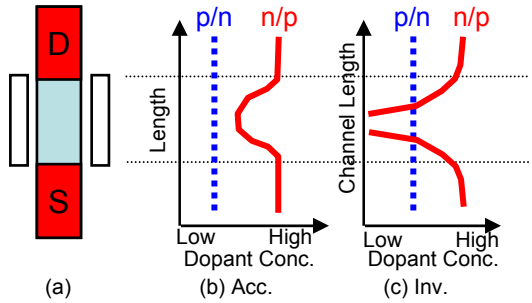

Fig. 1. (a) Schematic and (b) channel dopant distribution of an accumulation-mode and (c) an inversion-mode DG-MOSFET. In the accumulation mode, the channel conduction type is the same as that of S/D regions, while the opposite in the inversion mode.

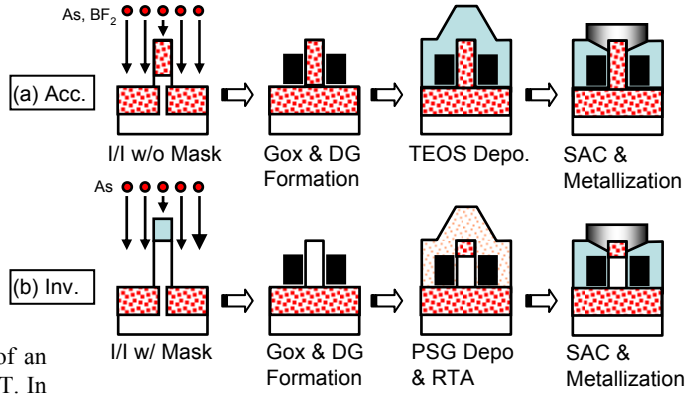

Fig. 2. Fabrication process flow of (a) an accumulation-mode and (b) an inversion-mode vertical DG-MOSFETs.

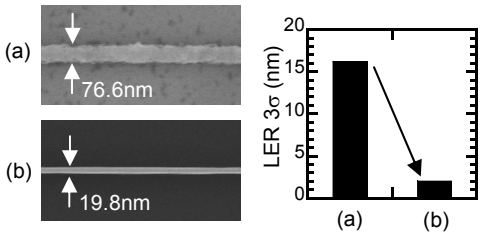

Fig. 3. Top-view SEM images and LER of (a) an EB resist just after development and (b) a vertical channel after orientation-dependent wet etching (ODWE). The ODWE successfully contributes to the improvement of the channel LER.

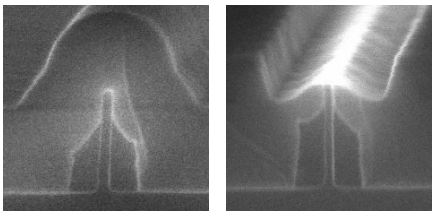

Fig. 4. XSEM images for each step of SAC opening: (a) after the TEOS deposition and (b) after the SAC opening.

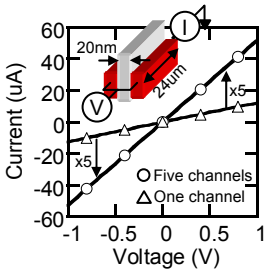

Fig. 5. I-V characteristics of the DGs formed on the both side of 20-nm-thick and 24-um-length vertical channel.

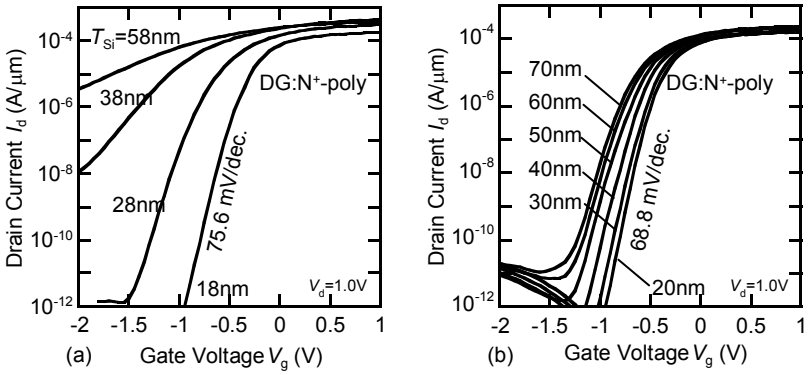

Fig. 6. Measured I_d-V_g characteristics for (a) the short-L_g accumulation-mode NMOS vertical DG-MOSFETs and (b) the long-L_g inversion-mode NMOS vertical DG-MOSFETs. In the accumulation-mode, the V_{th} drastically shifts to the negative as the T_{Si} slightly increases.

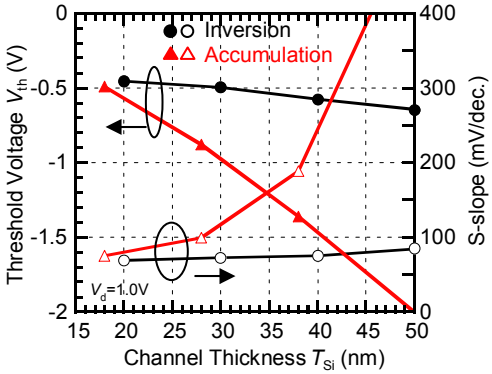

Fig. 7. Measured dependence of the V_{th} and s-slope on T_{Si}. In the accumulation mode, by decreasing T_{Si}, both the V_{th} and s-slope are improved to the same values as those for the long-L_g inversion-mode DG-MOSFET.

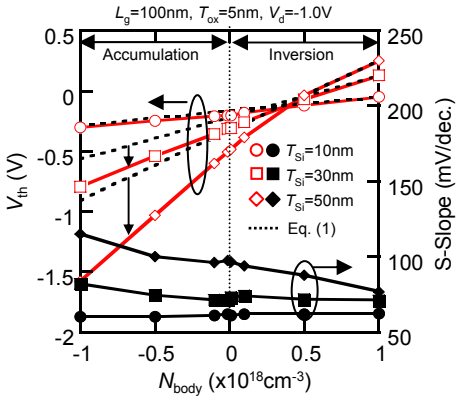

Fig. 8. Simulated N_{body} dependence on V_{th} and s-slope for NMOS DG-MOSFETs. If T_{Si} is sufficiently thin, the simulated V_{th} corresponds to that estimated Eq. (1) and s-slope maintains 60 mV/dec. regardless of N_{body}.

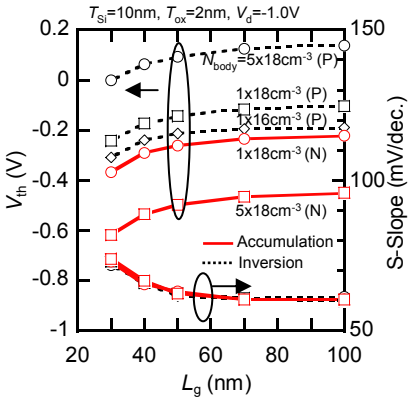

Fig. 9. Simulated L_g dependence on V_{th} and s-slope for the 10-nm-T_{Si} and 2-nm-T_{ox} NMOS DG-MOSFETs. Both the accumulation- and inversion-mode DG-MOSFETs show the same SCE trend.

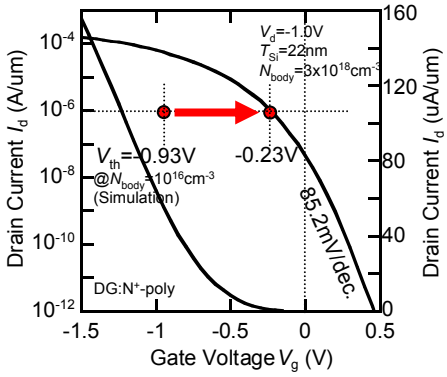

Fig. 10. Measured I_d-V_g curve of the accumulation-mode PMOS vertical DG-MOSFET with the n^+-DGs. An appropriate V_{th} as well as a low s-slope can be attained by use of the n^+-DGs and control of N_{body} and T_{Si}.