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Characteristics of Metal Gate GOI-MOSFET with High-*k* Gate Dielectric Fabricated by Ge Condensation Method

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1. Introduction

Ge has recently regained considerable attention, since Ge can provide solutions to overcome major roadblocks that Si technology is facing for advanced CMOS devices. This is mainly due to the higher mobility of both electron and hole in Ge-substrate. Meanwhile, a Si-On-Insulator (SOI) devices become extremely attractive because of the advantages in high speed, low power dissipation and extended scalability. In particular, a fully-depleted (FD) SOI CMOS are better candidate for low power applications due to its superior short channel immunity, low junction capacitance and steep substhreshold slope. Therefore, FD strained Ge-On-Insulator (GOI) MOSFET, which is the combination of strained Ge channel and FD-SOI MOSFET, is expected to achieve a higher CMOS performance as compared to conventional CMOSFET with Si channel. Recent work has demonstrated excellent capacitance-voltage characteristics from Ge MOS capacitors using high-*k* germanium oxynitride [1] and HfO_2 [2] for the gate dielectric. These very promising results suggest that the use of Ge channels will allow CMOS technology to be extended beyond the limitations imposed by the material properties of silicon. In addition, the metal gate electrodes such as W, TiN and Ta have been reported to be promising candidates to realize no gate depletion and low gate resistance [3]. Especially W/W_2N has several merits such as high thermal stability, good corrosion resistance, and mid-gap work-function (4.52eV). W_2N was introduced as barrier material. It is expected that the surface nitridation of the gate dielectric occurs during in-situ reactive sputtering deposition of W_2N layer. Thereby, the improvement of the gate dielectric reliability is achieved by the nitridation, which terminated the dangling bonds formed on the gate dielectric surface during the metal gate sputtering [4].

In this study, we have investigated Ge MOSFETs with HfO_2 gate dielectric and W/W_2N metal gate which are fabricated on GOI wafer obtained by the Ge condensation method.

2. Experiments

Ge layer was formed by the oxidation of a SiGe layer which was epitaxially grown on SOI wafer by ultra-high-vacuum chemical vapor deposition (UHV-CVD) varying the gas ratio of Si_2H_6/GeH_4. Using this method, it is expected that Ge is condensed during oxidation [5].

Throughout this research, the high-*k* dielectric (HfO_2) was deposited at 400°C and W_2N was deposited at 250°C by the RF magnetron sputtering system. W_2N film was deposited changing the amount of Gas (N_2) and the temperature of a substrate. As a merit of this research, HfO_2 and W/W_2N gate stack was continuously deposited in the same chamber of sputtering system. Therefore, impurities and contaminations were able to be minimized in the thin film. Consequently, excellent C-V characteristics were obtained in a MOS capacitor fabricated on Ge substrate with low leakage current.

3. Results

Germanium compositions of all films were measured by secondary ion mass spectroscopy (SIMS), atomic force microscope (AFM) and X-ray diffractometry (XRD). First of all, an optimal formation of GOI layer was investigated changing the condensation condition. Figures 1 and 2 show SIMS profiles before and after oxidation. In these figures, it is found that silicon is replaced by germanium after oxidation. In addition, Figure 1 shows that SiGe concentration changes with variation of gas flow (Si_2H_6/GeH_4) in the profiles before oxidation. Figure 3 shows an AFM image of the GOI layer after removing surface oxide. RMS values for surface roughness before and after oxidation are 3.80nm and 0.84nm, respectively. As shown in the figure, surface roughness characteristics are improved by dry oxidation. Figure 4 shows the XRD result of germanium and W_2N used for this research. As shown in this figure, Ge (111) peak is remarkable as a result of Ge condensation. It is positive proof to indicate that SiGe layer is changed to Ge layer, and it turns out that there is no W component and only W_2N exists.

The measured high-frequency C-V characteristic of n-MOS capacitor with $W/W_2N/HfO_2/Ge$ stack is shown in Figure 5. EOT of 7.83Å is achieved, along with excellent agreement of HFCV, indicating high quality of n-MOS capacitor with $W/W_2N/HfO_2/Ge$ stack.

Figures 6 and 7 show characteristics independently in the gate length of n-MOSFET. These figures exhibit well behaved I_d-V_d characteristics. Sub-threshold swings of 112mV/dec and 86mV/dec are obtained for n-MOSFET. Operational n-MOSFET with gate lengths down to 2.3μm

was fabricated. In this case the Ge layer has a thickness of 30nm. Electrical characteristics are shown in Figures 6 and 7. The transfer and output characteristics of an n-channel transistor with a gate length of about 2.3μm are given in Fig. 6. A very low leakage current below 1nA was achieved. The on-current of 75μA/μm at V_d=V_g=1.2V shows evidence of a high quality channel surface. Further enhancement of on-currents is anticipated by using a spacer optimization, or reducing the contact resistance (Nickel Germanide, LDD).

4. Conclusions

We have presented the advantages and the current status of strain Ge n-MOS device (EOT~7.83Å) fabricated with GOI substrate obtained by the Ge condensation technology, and using W/W_2N/HfO_2 gate stack. It is strongly expected that MOSFETs based on Ge can provide new device option to sub-100nm CMOS technology with high performance and low power consumption.

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References

[1] H. Shang, H. Okorn-Schimdt, J.Ott, P. Kozlowski, S. Steen, E. C. Jones, H. S. P. Wong, and W. Hanesch, *IEEE Electron Device Lett.,* **24** (2003) 242.

[2] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, *IEEE IEDM Tech. Dig.* (2003) 437.

[3] T. Yamada, M. Moriwaki, Y. Harada, S. Fujii, and K. Eriguchi, *Microelectron. Reliab.,* **41** (2001) 697.

[4] M. Moriwaki, T. Yamada, Y. Harada, S. Fujii, M. Yamanaka, J. Shibata, and Y. Mori, *Jpn. J. Appl. Phys.,* **39** (2000) 2177.

[5] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, *Appl. Phys. Lett.,* **83** (2003) 3516.

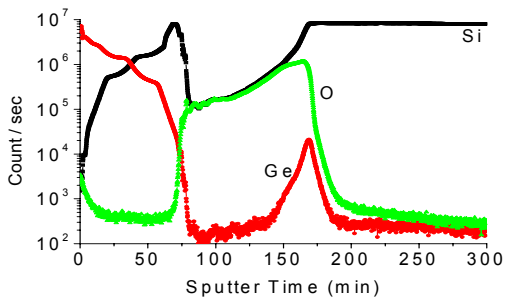

Fig. 1. SIMS profiles of GOI layer before oxidation

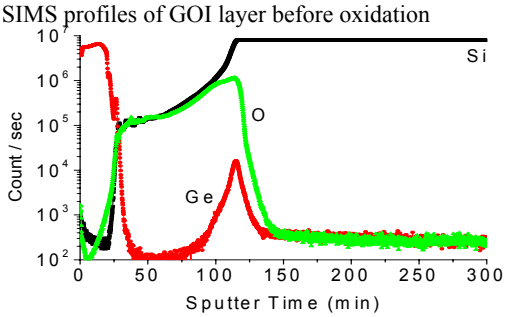

Fig. 2. SIMS profiles of GOI layer after oxidation

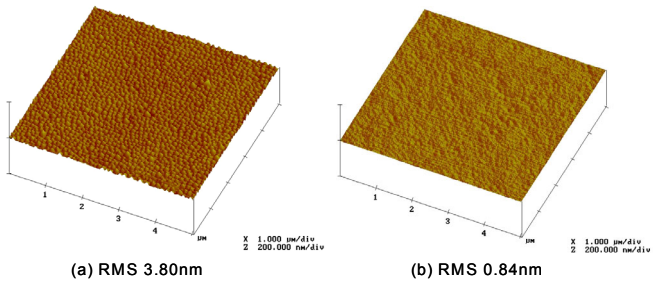

Fig. 3. AFM image of the GOI layer

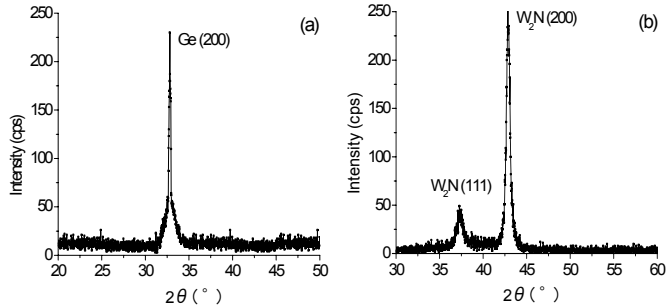

Fig. 4. The XRD result (a) after condensation and (b) W_2N

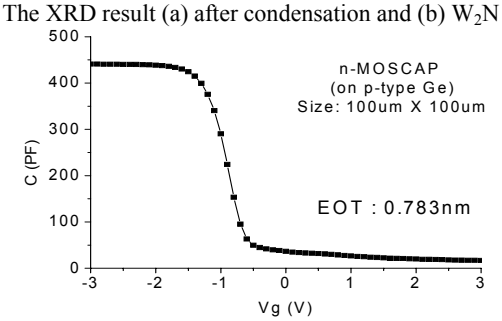

Fig. 5. Measured HFCV of n-MOS capacitor with W/W_2N/HfO_2/Ge stack

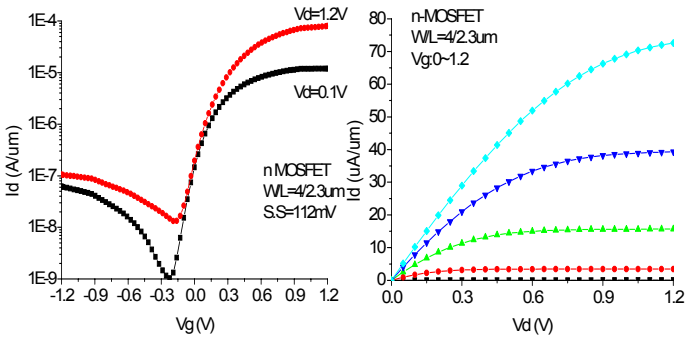

Fig. 6. I_d-V_g characteristics for Ge n-MOSFET with L_g of 2.3μm

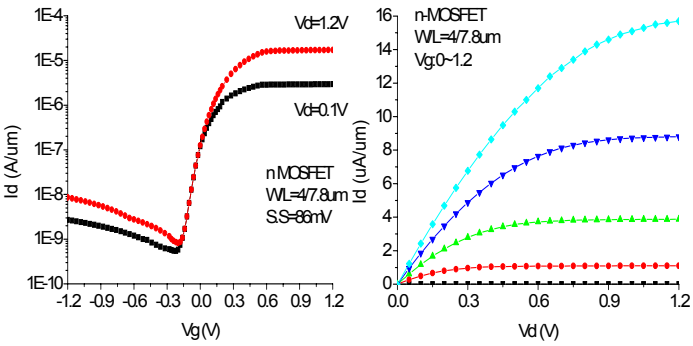

Fig. 7. I_d-V_g characteristics for Ge n-MOSFET with L_g of 7.8μm