P4-1

The New Technology for DRAM Cell Transistor with S-RCAT and its Size Effect

Se Geun Park[1,3], Ji Young Kim[1], Yong Il Kim[1], Ho Jin Oh[1,] Won Suk Lee[2], Ji Hye Kim[1], Sung Eui Kim[1], Myoung Sub Shim[1], Kyu Pil Lee[1], Yong Jik Park[1], Won Shik Lee[1], Byoung Il Ryu[1], and Yong Han Roh[3]

[1]Samsung Electronics, Advanced Technology Team , [2]CAE Team
Taean-Eup, Hwasung-city, Gyounggi-do, Korea
Tel) 82-31-208-2949, Fax) 82-31-208-2769, E-mail) onzenith.park@ samsung.com
[3]SungKyunKwan Univ. , School of Information & Communication Engineering
Chunchun-dong, Suwon-city, Gyounggi-do, Korea

1. Introduction

As the design rule of DRAM shrinks down below 100nm, the novel process technologies for DRAM integration have been proposed [1]. Recess-Channel-Array-Transistor (RCAT), which has been adapted from 110nm process technologies [2], is recently playing a major role in DRAM cell array transistors accompanying a remarkable improvement of data retention time, showing excellent product feasibility even down to 80nm node [3]. However, as the design rule shrinks further, the body effect and sub-threshold swing (SW) increase due to the sharp bottom profile of RCAT. It induces both threshold voltage (V_{th}) and SW to increase. To reduce the SW, Sphere-Shaped-Recess-Channel-Array-Transistor (S-RCAT) process has been introduced and the effects of the ball-diameter of the S-RCAT are evaluated. As the ball-diameter of S-RCAT increases, electrical characteristics such as drain induced barrier lowering (DIBL), SW, and body effect are improved. The comparison with RCAT and S-RCAT is carried out at the point of the data retention time with negative word line bias conditions.

2. Experiments and Results

A. Device Fabrication

DRAM using S-RCAT was integrated on p-type bulk Si (100) wafer and the process sequence is illustrated in Fig. 1. After formation of active region, hard mask layer is deposited. And the photo lithography patterns are formed on the deposited mask layer [Fig. 1a]. The upper neck part is formed by mask etch/Si recess etch processes as same as RCAT, followed by thin oxide deposition to form oxide spacer [Fig. 1b]. Spherical ball shaped area is made by isotropic dry etch process after thin oxide spacer forming [Fig. 1c]. Figure 1e shows finalized S-RCAT shape after ball formation followed by oxide removal by wet cleaning and followed gate stack. Table. 1 shows the experimental groups which are composed of different ball size. Wet oxidation process was used and n+ doped poly crystalline Si was then deposited, followed by gate stack patterning and ILD deposition. Figure 2 shows a successfully integrated DRAM structure using S-RCAT technology. TEM images are shown in Fig. 3.

B. Electrical Characteristics

As the ball-diameter increases, V_{th} is lowered with the same doping concentration [Fig. 4]. The doping concentration and profile at the active region are not changed; because the recessing etch processes were conducted after ion implantation processes forming active regions. The decrease of V_{th} is caused by the increase of the bottom curvature, which lowers the potential barrier at end points of curvature. As the ball-diameter increases, the volume of substrate Si which is controlled by a unit gate length is decreased [Fig. 5] [4]. It induces V_{th} to be decreased as C_{ox} increases although the effective channel length is increased. However, if the ball-diameter exceeds a critical point, V_{th} is not further lowered [Fig. 6]. The simulation result in Fig. 6 shows the same results. It is attributed to the saturated curvature improvement with the ball-diameter. The result that the V_{th} is lowered even if the channel length is increased is contrary to that of the planar transistor. Although V_{th} saturates as the ball-diameter increases, DIBL and SW are improved a little by the channel length increment effect as the ball-diameter increase [Fig. 7, 8]. However, I_{on} does not degrade as the ball-diameter increases because the reduction of I_{on} due to increment of L_{eff} is as same as the increment of I_{on} due to reduction of potential peak. In the RCAT, the Vth of cell transistors is kept over 1.18V to keep data retention time under word line disturbed test mode. However, in S-RCAT it is needed just 0.92V by low I_{off} characteristic caused from improved DIBL and SW. It leads to the improvement of the operating current, I_{on} from 3uA/cell to 6uA/cell [Fig. 9, 10]. Figure 11 shows the increase of word line capacitance (C_{wl}) by the ball-diameter increase.

C. Data Retention Time between S-RACT and RCAT

Recently, for reducing power consumption and improving dynamic retention time by lowering the word line operation voltage, NWL (Negative Word Line) has been used in DRAM devices [5]. However, the NWL degrades static retention time due to increasing GIDL, especially in RCAT structure [6]. Hence, in RCAT structure, it is difficult to use NWL scheme. S-RCAT with GWL scheme is the useful solution to lower the word line operating voltage without degradation of dynamic retention time due to lower off-current characteristics than R-CAT. We have compared the dynamic retention fail bits for S-RCAT with those for RCAT on the cell array transistor threshold voltage [Fig. 12~14]. With S-RCAT, high static retention time can be obtained by using GWL, high dynamic retention time also can be obtained due to low off-current characteristics, and low power consumption by using low word line voltage due to low V_{th}.

3. Conclusion

For the first time, DRAM devices with S-RCAT using the various diameters are successfully fabricated. It is found that ball-diameter of the S-RCAT determines V_{th}, DIBL, and SW. Adapting the S-RCAT technology, we can get lower cell transistor V_{th} and higher cell transistor I_{on} and lower cell transistor I_{off} than those for RCAT technology. The characteristics of S-RCAT improve both static and dynamic retention time and reduce the power consumption. S-RCAT will be one of the key technologies under 80nm DRAM architecture, especially for low power device like the mobile applications.

Reference

[1] K.N.Kim et al., *IEEE Trans. SM.*, vol.15, pp.137-143 (2002)
[2] J.Y.Kim et al., *Symp. on VLSI Tech.*, pp.11-12 (2003).
[3] H.S.Kim et al., *IEDM*, pp411-414, Dec.2003

[4] J.Y.Kim et al., *VLSI TSA*, April.2005
[5] J.Y.Sim et al., *Symp. On VLSI Tech*., pp.289_292
[6] Y.S.Kim et al., *Journal of the Korean Physical Society* (2004)

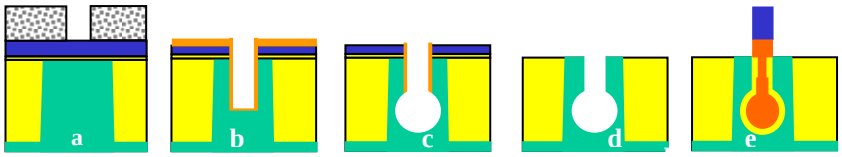

Fig. 1 Process sequences for S-RCAT structure. The core process is to make a spherical ball structure

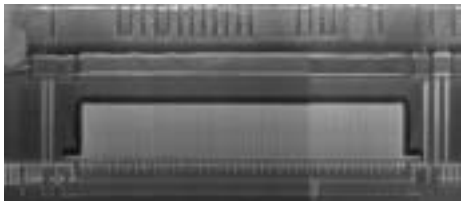

Fig. 2 fully integrated structure with S-RCAT.

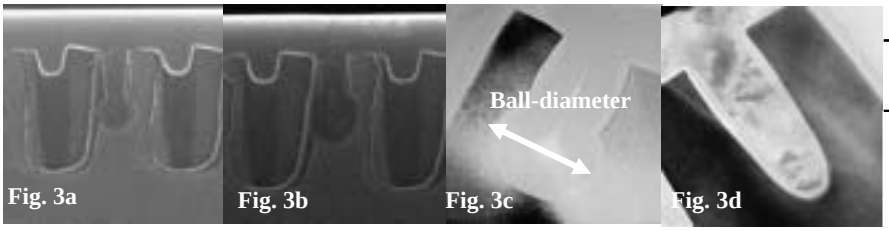

Fig. 3 S-RCAT VSEM and TEM Image
(3-a) 100nm ball size, (3-b) 140nm ball size, (3-c) 100nm ball size TEM, (3-d) RCAT TEM
S-RCAT shows uniform thickness without oxide-thinning problem.

Table.1 Experiment groups (nm)

	Diameter	Ball Depth	Neck Depth	Total Depth
A	80	85	100	185
B	100	90	95	185
C	140	110	75	185

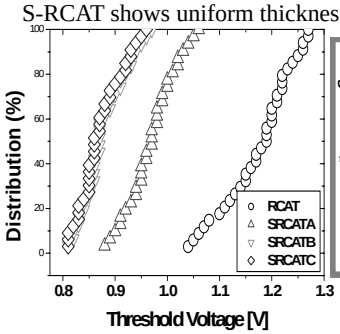

Fig. 4 Distribution curve of the V_{th}.

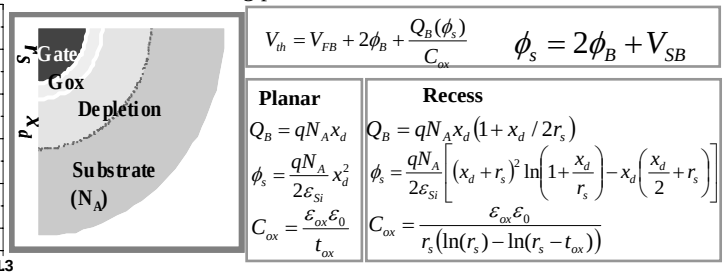

Fig. 5 Comparison of numerical expression for V_{th} between planar and Recess transistor.

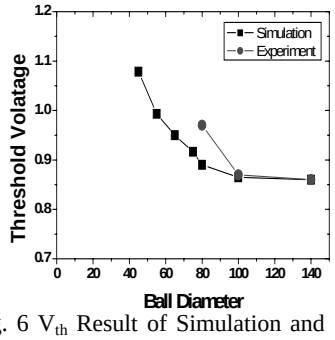

Fig. 6 V_{th} Result of Simulation and Experiment.

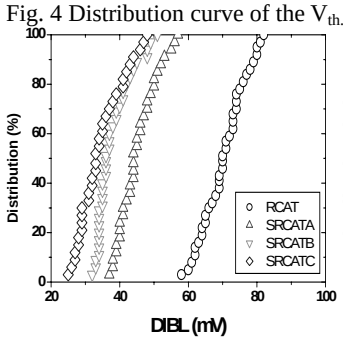

Fig. 7 Distribution curve of DIBL. DIBL is improved due to increased effective channel length.

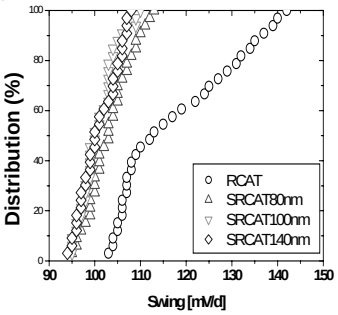

Fig. 8 Distribution curve of SW.

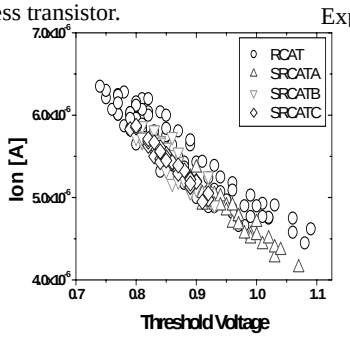

Fig. 9 Correlation plot between V_{th} and I_{on}. S-RCAT has I_{on} gain by 2 times more than RCAT.

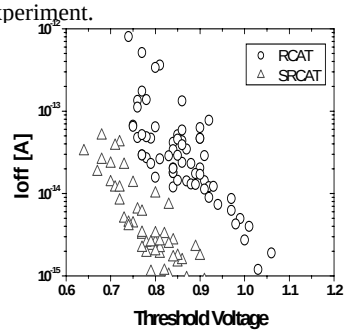

Fig. 10 Correlation plot between V_{th} and I_{off}. V_{th} of S-RCAT Could be lowered by 300mV.

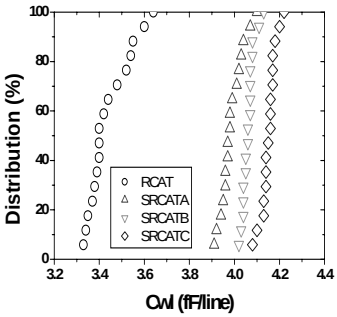

Fig. 11 as the diameter increase, C_{wl} increases due to increased surface area of gate oxide.

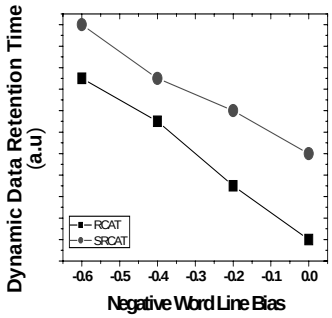

Fig. 12 Correlation plot between gate bias and dynamic data retention time.

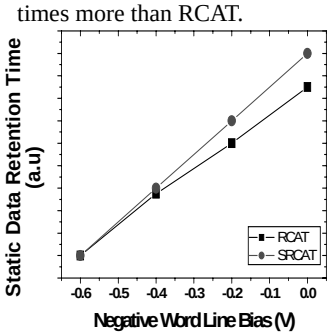

Fig. 13 Correlation plot between gate bias and static data retention time.

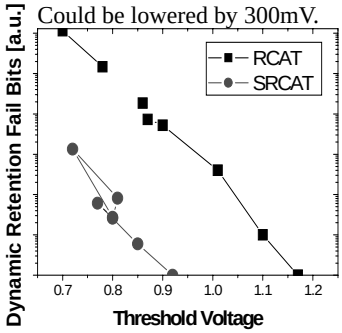

Fig. 14 Correlation plot between V_{th} and dynamic retention fail bits.