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Annealing effect of phase change and current control in phase change channel transistor memory

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1. Introduction

Electronic phase change random accessible memory (PRAM) has attracted much interest due to its promising merits.[1-2] The application of these devices is based on the ability of chalcogenides to be reversibly transformed between the highly resistive amorphous and lowly resistive crystalline phases by Joule heating.

The memory cell of PRAM consists of a transistor and a reversible resistor. By further simply putting the reversible resistor into the transistor, we proposed a novel phase change channel transistor memory.[3] Gate and drain electrodes can work as word line and bit line in the transistor memory cell, respectively. Thus two functions can be combined in a transistor: 1) nonvolatile memory based on phase change effect; 2) the selection of memory cells (current control) based on Coulomb blockade effect or field effect.

Crystal size smaller than 10 nm is required for Coulomb blockade effect at room temperature.[4] Hence, it's necessary to study devices with a thin chalcogenide film and demonstrate the two combined functions mentioned above using prototyped memory devices by annealing first.

2. Experimental

The schematic diagram of the transistor memory device samples is shown in Fig. 1(a). Figure 1(b) shows the atomic force microscopy (AFM) image of a device sample. 10 nm or 20 nm-thick $Ge_2Sb_2Te_5$ (GST) was sputtered using sputtering system (i Miller: Shibaura Mechatronics co., Ltd). The deposition rate was approximately 0.57 nm/s. Current-voltage (I-V) characteristics of device samples were measured by semiconductor parameter analyzer (4155B: Agilent Technologies, Ltd.) in air at room temperature. In the I-V measurements, tungsten (W) probes were used to contact on samples.

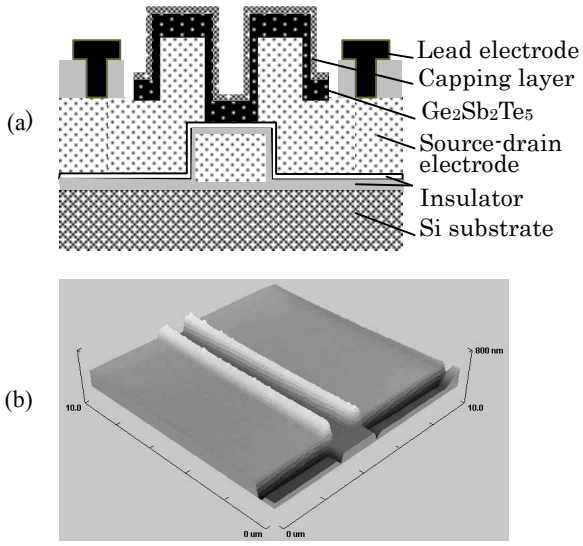

Fig. 1 (a) Schematic cross section diagram of the device sample (b) The 3-dimentional AFM image of a device sample.

3. Results and discussion

Demonstration of phase change by annealing

Samples were annealed at temperatures from 127 °C to 235 °C for 2 min. Figure 2 shows two typical I-V

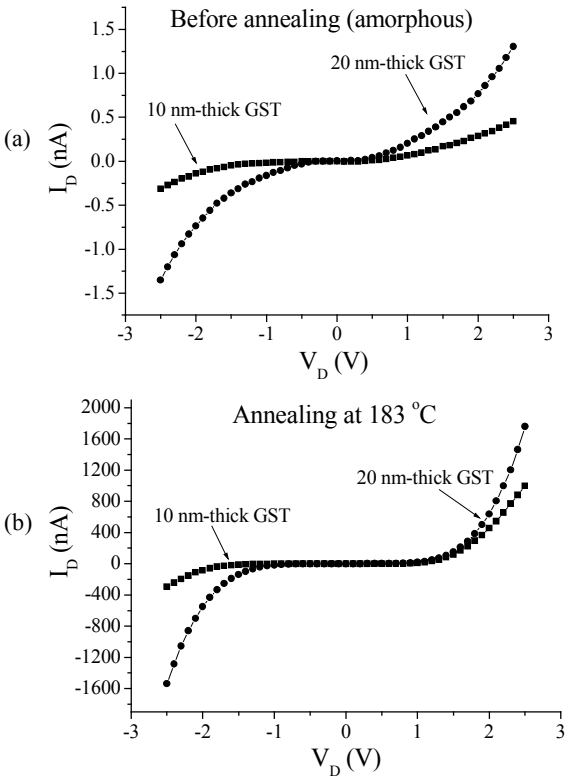

Fig. 2 Typical I-V characteristics of GST memory device samples (a) before and (b) after annealing at 183 °C.

characteristics of the device samples before and after annealing in a drain voltage from –2.5 V to 2.5 V. The devices shown in Fig. 2 have a channel length of 1.0 μm and a channel width of 7.0 μm.

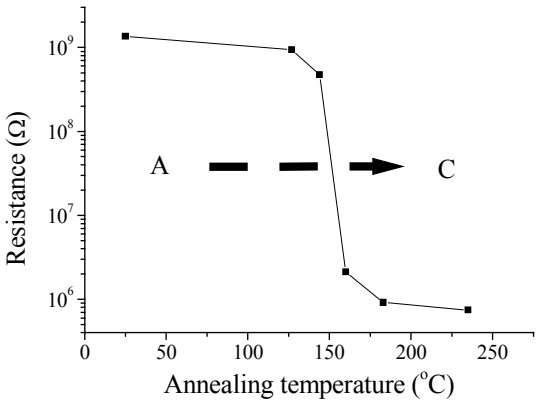

Fig. 3 Typical resistance vs. annealing temperature which shows that phase change from amorphous to crystalline.

The source-drain resistances of the device samples have been roughly calculated at a voltage of 2.5 V. Typical resistance versus annealing temperature was plotted in Fig. 3. Resistance decreases a little at 127 °C and 144 °C while it suddenly decreases from several 10^8 to 10^6 Ω at 160 °C. The sudden decrease in resistance was caused by phase transformation from amorphous (high resistance) to crystalline (low resistance), which can be used for nonvolatile memory. The crystallization temperature T_x when annealing for 2 min is about 150-160 °C.

Demonstration of current control by annealing

Crystallization is a process of nucleation and crystal growth. By annealing at a temperature a little lower than T_x with time, a more detailed transition can be obtained. Current control with crystal growth is thus available for channel current control.

Figure 4 shows current control effect of a 10-nm thick GST device at a drain voltage of 3 V when GST is amorphous and partially crystalline. At a given gate voltage, drain current increase with annealing duration, which is attributed to crystallization of GST chalcogenide channel. Current control effect becomes much stronger after annealing at 135 °C for 15 min, compared with that before annealing.

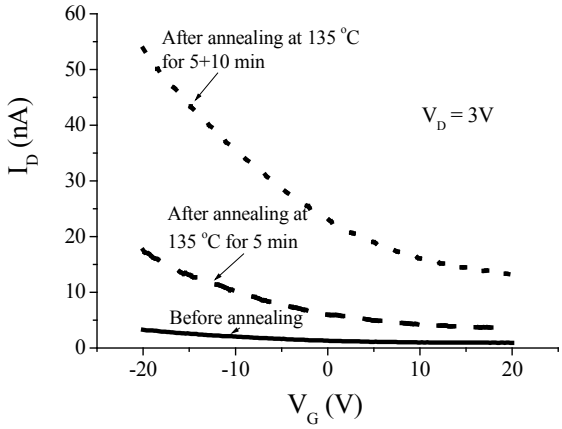

Fig. 4 Current control effect of a 10-nm thick GST device before annealing (amorphous) and after annealing at 5 min and 15 min (crystalline).

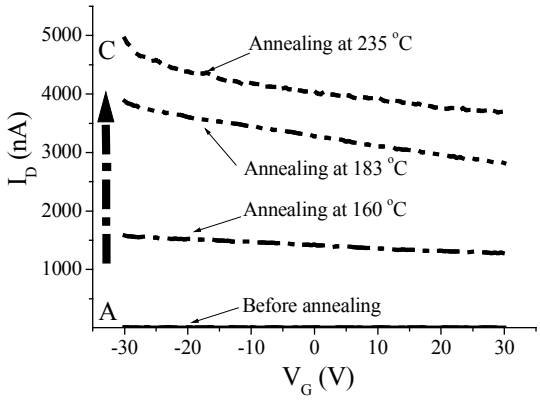

Fig. 5 Current control effect of a 20-nm thick GST device before and after annealing at 160 °C, 183 °C, 235 °C for 2 min.

On the other hand, we can also anneal the devices at increasing temperature but for a certain time. One typical of current control effect of GST devices at a drain voltage of 3 V before and after annealing at various temperatures for 2 min is shown in Fig 5. After annealing at 183 °C and 235 °C, drain current can be significantly controlled by changing gate voltage compared with that before annealing.

4. Conclusions

Based on measured electrical properties of 10 nm and 20 nm-thick GST transistor memory devices, conclusions can be drawn as below.

(1) Source-drain resistance can be changed due to annealing by about 2-3 orders of magnitude based on phase change effect, which can be used for nonvolatile memory.

(2) After crystallization of chalcogenide channel, a much stronger current control effect could be obtained, which can be used for cell selection in a memory array.

(3) The combination of the above two functions (nonvolatile memory and cell selection) is demonstrated by annealing.

(4) The current control effect in 10 nm-thick GST devices is stronger than that of 20 nm-thick GST devices.

Acknowledgements

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