# Ultra High Density HfO2-Nanodot Memory for Flash Memory Scaling

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# Abstract

We have developed a simple technique for forming ultra high density  $HfO_2$  dots with diameter < 3 nm and density >  $5x10^{12}$  cm<sup>-2</sup>. Advantages of our method are that the density and diameter are controllable and the dots are well separated with average space 3 nm between dots. We propose that the ultra high density dots are suitable for charge storage node in the future 45 and 32 nm generation Flash memory.

## **1. Introduction**

For further scaling of flash memory technology, discrete charge trap memories with nanocrystals or nano-dots have been studied widely [1]. The reliability problems of thinner tunnel oxide is partly compensated with discrete trap layers as well as lower gate stack structure decreases the electric filed coupling interference with neighbor gates. Most of the reported nano-particle densities are up to lower  $10^{12}$  cm<sup>-2</sup>. For the case of  $1 \times 10^{12}$  cm<sup>-2</sup> density, average 5 particles locate along a 50 nm gate span. For large scale flash memory, this density is not enough due to a large variation of nanoparticle numbers in gate regions.

In this paper, we fabricated the mid- $10^{12}$  cm<sup>-2</sup> density HfO<sub>2</sub> dot and confirmed the program and erase flash memory operation into HfO<sub>2</sub> dots. Charge hopping between HfO<sub>2</sub> dots is suppressed comparing with lateral charge migration in the planar HfO<sub>2</sub> trapping layer.

## 2. Preparation of HfO2 nanodots

High density HfO2 dots were formed with selfagglomeration of HfO2 thin layers. HfO2 layer is well known to form nanocrystals with high temperature annealing above 800C. HfSiO films shows phase separation into HfO2 nanocycrystals and SiO<sub>2</sub> layers with high-temperature annealing, too. We used these characteristics to make high-density and very small nanodots of HfO2. First, 0.5-2nm thick HfO2 thin layers were deposited by metal-organic chemical vapor deposition (MOCVD) on SiO<sub>2</sub> layers. With the rapid thermal annealing (RTA) above 1000C, HfO2 thin layer starts to agglomerate to form nanodots. Then CVD SiO2 were deposited to fill the space between nanodots (Fig.1). TEM observation of nanodots (Fig.2) confirms that the average 2-nmdiameter nanodots are formed (Fig.3) and its sheet density is as large as  $6x10^{12}$  cm<sup>-2</sup>. This number is roughly one order of magnitude larger than conventional Si nanocrystals. We found that the diameter and the density of nanodots depend on the thickness of the initial HfO2 thin layer (Fig.4). Below 1 nm HfO<sub>2</sub> layer thickness, high density HfO<sub>2</sub> dot can be formed with the RTA. During the RTA process, nascent  $HfO_2$  small nanodot does not have enough time to collide with each others to form larger dots. For the 2 nm  $HfO_2$  layer, self-agglomeration is not occurred and a planar film was observed by TEM (Fig.5).

These densities are much larger than the HfO<sub>2</sub> dot density in HfSiO phase separation, too [2]. This is the advantage of the use of self-agglomeration. We can expect that the HfO<sub>2</sub> nanodots are capable for well defined flashmemory operation with several tens nm gate length. In Fig. 2 b), we compare the gate feature sizes of 45/32 nm with a plane-view TEM. The number of nanodots in the gate areas is enough for stable operation even with the scattering nature of the nanodot formation.

## 3. Flash memory operation

We fabricated the MONOS-type flash memory with HfO<sub>2</sub> nanodot charge traps (Fig.6). Fig. 7 shows the channel hot electron programming and hot hole erasing characteristics of this device. 2-bit/cell operation is confirmed. Microseconds' programming speed and 100  $\mu$  s erasing speed are obtained. Fig.8 shows the advantage of nanodots over the planar trapping layer. In the previous work, the lateral migration of the trapped electrons is very prominent in the HfO<sub>2</sub> layer (Fig. 8 a)) [3]. With the nanodot formation, this lateral migration or charge hopping are suppressed effectively (Fig.8 b)). High density HfO<sub>2</sub> nanodot memory is one of very promising candidates for further scaling of flash memory beyond 45 nm.

#### 4. Summary

Ultra high density HfO<sub>2</sub> nanodots up to Mid- $10^{12}$  cm<sup>-2</sup> density were fabricated adopting self-agglomeration of HfO<sub>2</sub> thin layer with RTA. The program and erase operations of HfO<sub>2</sub> nanodot charge traps were confirmed. With the nanodot formation, the lateral migration of trapped charge is suppressed effectively. Ultra high density HfO<sub>2</sub> dots memory is very promising to further scaling of flash memory technology.

#### References

- [1] S. Tiwari et al., IEDM Tech. Dig., 521 (1995).
- [2] Y.H. Lin et al., IEDM Tech. Dig., 759 (2004).
- [3] T. Sugizaki et al., Symp. On VLSI Technol., 27 (2003).





Fig.1 HfO<sub>2</sub> nanocrystal formation with self-agglomeration.





10 nm

Fig.2 HfO<sub>2</sub> nanodots observation. Thickness of as-deposited HfO<sub>2</sub> film is 0.5nm. a) Cross-sectional TEM image. b) Plane-view TEM photograph. Average sheet density of nanodots is  $6 \times 10^{12}$  cm<sup>-2</sup>. HfO<sub>2</sub> dot distribution and gate feature sizes are shown. For the clarity, each dot is marked with an open circle.



Fig. 3 Histogram of nanodot diameters. Average size is 2nm.



Fig. 4 Average nanodot density and diameter variations with deposited HfO<sub>2</sub> layer thickness. Open circles are average dot densities and closed circles are average dot diameters.

Tunnel oxide

HfO<sub>2</sub> film deposition

HTO deposition

anneal

Poly-Si

RTA for agglomeration



Fig. 5 Cross-sectional TEM observation for HfO<sub>2</sub> layer after RTA. The deposited HfO<sub>2</sub> film thickness is 2-nm.



Fig.6 HfO<sub>2</sub> nanodot flash memory structure.a) Schematic device structure.b) Process sequence.





Fig. 7 Program and Erase characteristics of HfO<sub>2</sub> nanodot memory. a) Vth increase with the programming pulse. Vg = 9 V and Vd = 5 V.  $\Delta$  Vth is the Vth difference from the fresh device. b) Vth decrease with the erase pulse. At the beginning, Bit "0" is programmed with 10  $\mu$  s pulse at Vg = 9 V and Vd = 5 V. The erase pulse condition is Vg = -8 V and Vd = 5 V.  $\Delta$  Vth is the Vth difference from the fresh device.

Fig.8 Comparison of charge loss characteristics of 2bit/cell type flash memory at room temperature. Lg = 0.25  $\mu$  m.: a) Planar HfO<sub>2</sub> trapping layer [3] and b) HfO<sub>2</sub> nanodot trap.